On heating rates in cryogenic surface ion traps.

M.Sc. Kirill LAKHMANSKIY

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Abstract

Systems based on trapped ions are promising candidates for the realization of large-scale quantum computation and quantum simulation. In particular, microfabricated surface electrode traps are a convenient approach to scale up ion traps. However, the proximity of the ions to the trap surface leads to an increased heating rate of the motional state. This limits the quality of operations and makes complex algorithms difficult to realize. The origin of this heating is not well understood. This work is centered around improving the understanding of sources of the ion heating rate.

In the first project we operate a surface ion trap made of yttrium barium copper oxide (YBCO), a high-temperature superconducting material, in order to investigate different sources of motional heating. The trap is designed in such a way that Johnson noise is the dominant source above the critical temperature $T_\mathrm{c} \sim 90\,\mathrm{K}$, while in the superconducting regime, Johnson noise should be negligible compared to other noise sources. Below the transition temperature, we measure surface noise spectra that deviate from a power-law dependence. Such noise spectra are generally expected and predicted, e.g. by two-level fluctuator models.

The second project is a study of silicon-based surface ion traps. We designed and fabricated surface ion traps with electrode-ion separation ranging from 50 µm to 230 µm. In these traps, we observed a light-induced charge carrier effect which creates a significant obstacle to trap operation. Namely, charge carriers in the bulk silicon lead to a drifting electric stray field.

Kurzfassung

Systeme, die auf gefangenen Ionen basieren, sind vielversprechende Kandidaten, um Quantencomputer und -simulatoren zu konstruieren. Insbesondere mikrofabrizierte Oberflächenionenfallen eignen sich gut, um skalierbare Quantencomputer zu realisieren. Der geringe Abstand zwischen Ionen und Fallenoberfläche in solchen Fallen führt allerdings zu hohen Heizraten der Bewegungsmoden. Dies limitiert die Qualität der Quantenoperationen und macht die Realisierung komplexer Algorithmen schwierig. Die Ursachen dieser Heizraten sind nicht im Detail verstanden. Diese Arbeit soll das Verständnis über die Heizmechanismen verbessern.

In einem ersten Projekt betreiben wir eine Oberflächenionenfalle, hergestellt aus dem Hochtemperatursupraleiter Yttrium-Barium-Kupferoxid (YBCO), um verschiedene Heizmechanismen zu untersuchen. Die Falle ist so entworfen, dass Johnson-Rauschen oberhalb der Sprungtemperatur von $T_\mathrm{c} \sim 90\,\mathrm{K}$ dominiert. Im supraleitenden Zustand ist Johnson-Rauschen gegenüber anderen Rauschquellen vernachlässigbar. Unterhalb der Sprungtemperatur messen wir eine Abweichung des Oberflächenrauschspektrums von einem einfachen Potenzgesetz. Eine derartige Abweichung wird im Allgemeinen erwartet und vorhergesagt, z. B. für Fluktuationen in Zwei-Niveau-Systemen.

In einem zweiten Projekt werden auf Silizium basierende Oberflächenionenfallen charakterisiert. Wir haben Fallen mit Abständen zwischen Chipoberfläche und Ion im Bereich zwischen $50\,\mu\mathrm{m}$ und $230\,\mu\mathrm{m}$ entworfen und hergestellt. In diesen Ionenfallen konnten wir Licht-induzierte Ladungsträgereffekte beobachten, welche das Speichern von Ionen stark erschwerten. Insbesondere führten Ladungsträger im Silizium-Substrat zu zeitlich veränderlichen elektrischen Streufeldern.

Contents

CHAPTER 1

Introduction

Over just the past decades, computers and information technologies have become essential parts of modern infrastructure and daily life. As of 2019, 5.13 billion people (from a total population of 7.73 billion people) have smartphone devices, when the first mobile phone was released only in 1983. To achieve higher computational power for the same chip size, manufacturers have succeeded in progressively reducing the size of the "building blocks" (transistors) of microprocessors. This behaviour is empirically described by Moore's law [1]. However, physics limitations, such as the gate leakage current, will soon prevent further reduction in the size of transistors. Thus, alternative ways to increase the performance of computations have to be found. One can think about computers based on completely different physics.

In 1982 Richard Feynman [2] and Paul Benioff [3] proposed to use quantum mechanical systems for simulation and computation. The main difference between such quantum mechanical simulators and computers and classical computers is a different realization of the fundamental unit of information. The bit of classical information can take the values 0 or 1. A quantum computer utilizes quantum mechanical two-level systems (qubits), which can be in any quantum mechanical superposition of $|0\rangle$ and $|1\rangle$.

Ion traps are one of the most promising available experimental tools to perform quantum

simulation [4] and quantum computation [5]. With conventional linear Paul traps, it is possible to store and manipulate tens of ions with high precision. Nevertheless, in order to achieve large-scale quantum systems, it will be necessary to hold and control more ions than is possible with conventional Paul traps. Surface ion traps offer one potential solution. Modern fabrication capabilities allow us to produce microchips with multiple trapping zones. For such surface traps to be useful for quantum computing, ions need to be placed close enough to each other in order to interact with one another by means of the Coulomb force, as such interactions are the basis for multi-ion logical gate operations. To scale up the number of confined ions in the trap, reduction of the size of electrodes is required, resulting in smaller electrode-ion separation. In turn, the closeness of the ions to the trap's surface leads to an increase of the heating rate of the ions' motional state, which degrades the fidelity of quantum operations. The origin of this heating is not well understood [6].

The first project of this thesis consists of an investigation of different sources of motional heating in surface ion traps. We use a trap made of the high-temperature superconducting material YBCO. The trap works in two distinct regimes, above and below the critical temperature T_c of its superconducting electrodes. Above T_c, an ion in the trap experiences a heating rate which originates primarily from the bulk properties of the trap's electrodes. In this regime, we demonstrate that our setup can be used to measure the resistivity of the superconductor in a non-invasive way, that is, we observe the superconducting transition without direct electrical probing. Below T_c, the resistance of these electrodes vanishes, and the ion probes the noise from the surface of the trap. In this regime we measure surface noise with a deviation from a power-law dependence in the frequency domain. Such a crossover regime between two different power-law exponents is generally expected [7] and predicted by two-level fluctuator (TLF) models [8, 6].

The goal of the second project of this thesis was to scale down surface ion traps fabricated on a silicon substrate. A previous PhD student, Michael Niedermayr, suggested a new fabrication approach for surface ion traps, based on microelectromechanical systems (MEMS) technology [9]. The approach is as follows: the substrate for trap chips is made of undoped (intrinsic) silicon which is patterned by deep reactive ion etching (DRIE). The electrodes of the trap are made of gold and confine the ion at a distance of 230 µm from the chip surface. To ensure operability, these silicon traps need to be cooled to below roughly 25 K, the temperature at which silicon turns from a semiconductor to an almost perfect insulator. The surface ion traps fabricated with this method allowed us to achieve a new record for ion trap heating rates, measured to be as small as 0.33 phonons/s [9]. As a

next step, during my thesis research, my colleagues and I wanted to exploit this promising fabrication technique to produce smaller traps for quantum computation. We simulated and designed new silicon-based traps with electrode-ion separations between 50 and 230 micrometers. We performed several fabrication runs. For the first run, we collaborated with Dr. Edlinger's team at the Fachhochschule (FH) Vorarlberg in Dornbirn, Austria. Dr. Edlinger's team patterned the silicon substrate, and we applied the final gold metallization. Such chips often exhibited electrical break-down. Nevertheless, with these chips it was possible to trap an ion 150 µm above the surface and to measure the ion's motional heating rate. We found that the behaviour of these ion traps was linked to charge generation in the bulk of the silicon caused by external light radiation. In an additional test, we reproduced the charge generation effect in the trap with 230 µm electrode-ion separation. Another goal of the project was to investigate the dependence of the ions' heating rates on the electrode-ion separation in the silicon traps. In these investigations, we made multiple attempts to use surface ion traps with an electrode-ion separation smaller than 150 µm but unfortunately, we did not succeed, due to technical difficulties and charge generation effect. In our second fabrication run, we collaborated with Infineon Technologies AG in Villach, Austria. The Infineon engineers carried out all necessary steps of the chip fabrication. With these chips, we verified the charge generation effect. We also performed RF and DC studies of the silicon substrate in the presence of an external light source.

This thesis consists of eight chapters. The underlying theoretical concepts are covered in chapter 2, which discusses the confinement of a charged particle by the combination of DC and RF fields in a Paul trap, the possibility of scaling up Paul traps to confine more ions, and the fundamentals of the level structure of $^{40}Ca^{+}$. Chapter 3 covers different aspects of ion motional heating rate. Detailed information about the experimental apparatus is given in chapter 4. Chapter 5 presents experiments with high-temperature superconducting surface ion traps. Chapter 6 discusses silicon-based surface ion traps. Chapter 7 summarizes the results presented in this thesis. Finally, additional information about electric field noise spectra of the technical noise related to chapter 5 and the details of a side project with a trap from Seoul National University (SNU) are given in chapter 8.

CHAPTER 2

Basics of ion trapping with linear Paul traps

$^{40}Ca^{+}$ ions confined in linear surface traps play a central role in this thesis. In 1953, Wolfgang Paul developed the mass spectrometer [10] which later evolved into the linear Paul trap. Such traps can hold tens of ions and have been the workhorse of trapped-ion quantum information processing. Yet in order to scale up the number of ions, one has to employ surface ion traps, based on microfabrication technology. This chapter discusses the theoretical background of techniques which are essential for trapping an ion. The first section is devoted to the basics of radio-frequency ion traps followed by specific details of $^{40}Ca^{+}$ and additional information about micromotion and ion-light interaction at the end of this chapter.

2.1 Basics of radio-frequency ion traps

The linear Paul trap allows us to confine charged particles, such as ions, in three dimensions. In the ideal theoretical case, the radial (x, y axis) confinement is provided by four hyperbol-

ically shaped electrodes (depicted as a gray rods in Figure 2.1) to which a radio-frequency (RF) voltage $V_{\mathrm{RF}} = \pm V_0 \cos \Omega t$ is applied to diagonally opposite pairs. The direct current (DC) voltage applied to the endcaps (blue electrodes in Figure 2.1) of the trap generates axial (z axis) confinement.

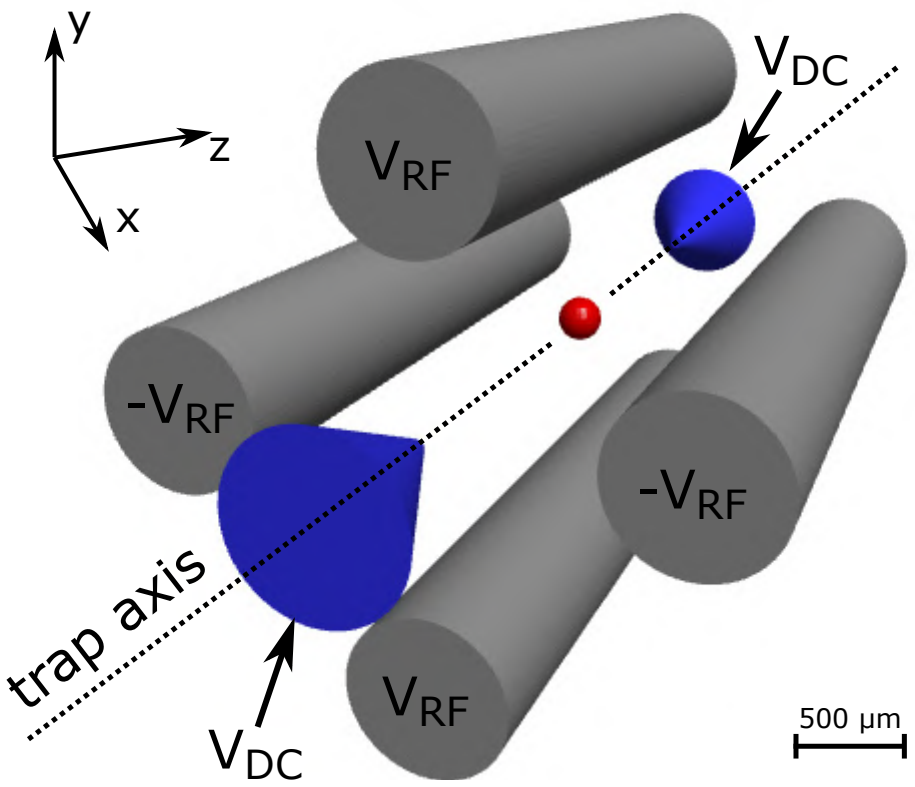


Figure 2.1: Schematic picture of the linear Paul trap. Grey rods depict hyperbolically shaped electrodes, which produce radial confinement (orthogonal to the trap axis). Blue electrodes (endcaps) on the sides are used for axial confinement. The red sphere in the center represents a trapped ion.

Let us consider how the RF voltage creates confinement in the (xy) plane. The RF voltage applied to the rods creates a 2-dimensional time-dependent quadrupole field given by

$$\Phi(x,y,z,t) = \left(\frac{x^2 - y^2}{d^2}\right) V_{\mathrm{RF}} \cos \Omega t, \tag{2.1}$$

where d is the minimum distance between one of the RF electrodes and the trap axis; see

Figure 2.1. Therefore, the motion of the ion (red sphere in Figure 2.1) can be described by two differential equations [11]

$$\frac{d^2x}{dt^2} - 2qt\frac{\Omega^2}{4}\cos(\Omega t)\,x = 0 \tag{2.2}$$

$$\frac{d^2y}{dt^2} + 2qt\frac{\Omega^2}{4}\cos(\Omega t)\,y = 0 \tag{2.3}$$

$$\frac{d^2z}{dt^2} = 0, \tag{2.4}$$

which are called Mathieu's equations and where q is the stability parameter for an ion with charge Q and mass m, given by

$$q = \frac{2QV_{RF}}{md^2\Omega^2}. \tag{2.5}$$

In order to achieve stable trapping of the ion, the q parameter has to satisfy $0 < q < 0.908$ [12]. The solution of Mathieu's equations (2.2) are two oscillating motions around the trap center.

The first solution is called secular motion with frequency $\omega_r = \omega_y = \omega_x = \Omega\frac{q}{2\sqrt{2}}$. This solution describes an ion slowly moving in a pseudopotential ($U_p(\vec{r})$) given by

$$U_p(x,y,z) = \frac{Q^2}{4m\Omega^2}\left|\nabla\Phi_{\text{eff}}(\vec{r})\right|^2, \tag{2.6}$$

where $\Phi(\vec{r})$ is the potential of equation (2.1) where $\cos\Omega t = 1$ [12]. Therefore, rewriting equation (2.6) yields

$$U_p(x,y,z) = \frac{V_{\text{RF}}^2Q^2}{4m\Omega^2d^4}(x^2+y^2). \tag{2.7}$$

For the case when d is smaller than the length of the RF electrode, the RF field creates a pseudopotential tube which induces confinement of the ion in the (x-y)- plane. When a DC voltage is applied to the endcaps (Figure 2.1), the ion is also confined in the z- plane with the quadrupole potential.

The second solution of the Mathieu's equations (2.2) is called micromotion and determined by the frequency Ω of the RF drive . The amplitude of such oscillations depend on how far the ion is displaced from the RF null (where the pseudopotential has its minimum). Stray fields can also effect the position of the ion. The effect of such unwanted micromotion of the ion results in Doppler shifts, as well as reduced cooling efficiency. In order to

minimize micromotion, one has to cancel out stray fields, which is achieved by means of additional DC voltage applied to the endcaps.

2.2 Scalable ion traps

In order to scale up Paul traps, one can use linear surface ion traps. Surface ion traps are based on microfabrication techniques that can produce micron-scale structures in a precise and reliable way, it allow us to have multiple trapping sites on the chip. And since ions, confined in different trapping sites, are oscillating charged particles they can interact with each other by means of the Coulomb force. The electrodes of a conventional Paul trap (Figure 2.1) can be modified and placed on a plane; see Figure 2.2.

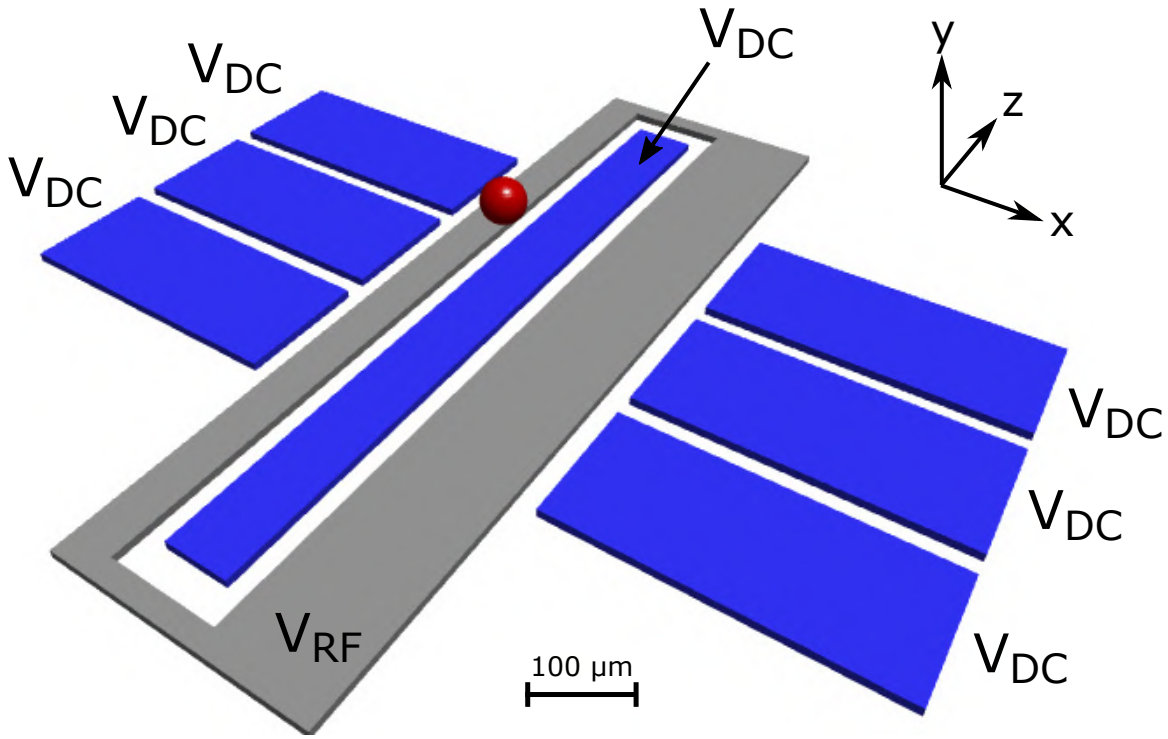


Figure 2.2: Schematic picture of the surface ion trap. The RF electrode, depicted in grey, produces radial confinement. The DC electrodes, depicted in blue, used for axial confinement. The red sphere in the center represents a trapped ion.

For this thesis, we use surface ion traps with an identical design concept using two RF electrodes connected together and seven DC electrodes. Three pairs of DC electrodes

placed on the sides of the RF electrodes and one central DC electrode are used to create a saddle potential for ion trapping (see Figure 2.3 (2)) and to shuttle the ion in the horizontal plane. Furthermore, it is possible to create several trapping regions if more DC electrodes are added on the side. The orientation of the radial axes is determined by the DC potential. Hence, the radial axes can be tilted versus y-axis (see Figure 2.3 (1)) such that efficient Doppler cooling of all motional modes can be achieved.

The two RF electrodes have different widths and are separated by the central DC electrode. The fact that the RF electrodes have a finite length leads to a non-ideal quadrupole potential as described in section 2.1. However, in close proximity to the RF minimum we can consider the potential produced by the finite electrodes to be harmonic.

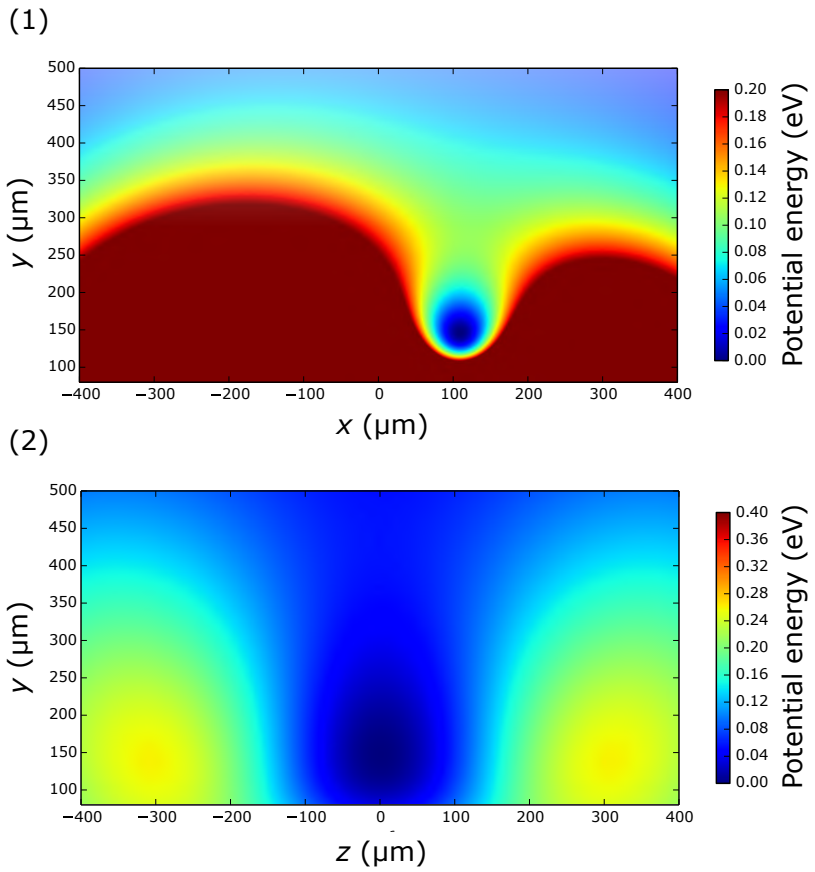


Figure 2.3: The pseudopotential (1) and the saddle potential created by the DC voltages (2) applied to the silicon trap chip with 150 µm ion-surface separation; see section 6.6.

2.3 Fundamentals of the $^{40}Ca^{+}$ ion

$^{40}Ca^{+}$ ions confined in Paul traps are used in all experiments presented in this thesis. $^{40}Ca^{+}$ is an alkaline-earth isotope with zero nuclear spin and thus has no hyperfine structure. The atom is ionized by means of two lasers, using a process that is explained in detail in section 4.4. The ionized calcium atom has a similar level structure as hydrogen because it has only one electron in the outer orbital.

The lowest energy level of the calcium ion is the $4^2S_{1/2}$ state; see Figure 2.4 (1). Then comes a metastable D-orbital with two fine structure levels $3^2D_{5/2}$ and $3^2D_{3/2}$ which are energetically split by spin-orbit coupling. Both of these states have a lifetime of more then a second. Hence, an optical qubit is realized on two calcium states: the ground state is $4^2S_{1/2}$ and excited state $3^2D_{5/2}$ with long lifetime. A narrow bandwidth laser at 729 nm is used to induce this transition.

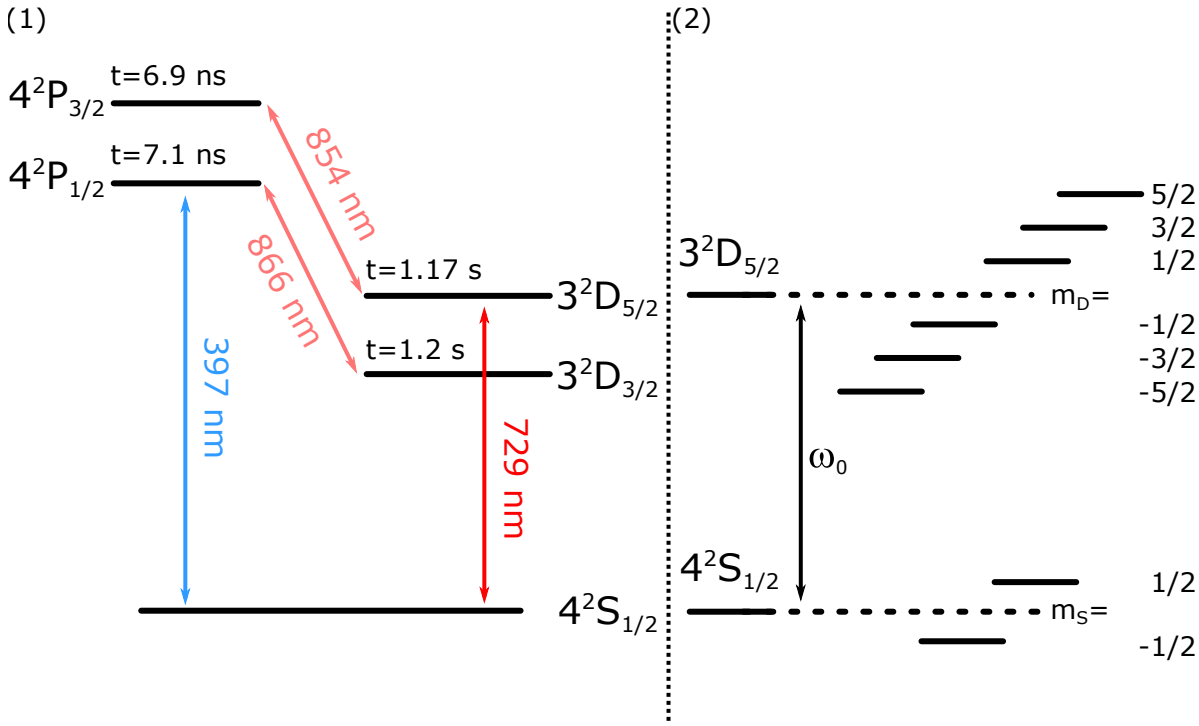


Figure 2.4: (1) The basic level scheme of $^{40}Ca^{+}$, simplified for the needs of this thesis. (2) Zeeman sublevels of D- and S-orbitals in the presence of a magnetic field B. The D-orbital is split into six levels and the S-orbital into 2 levels.

The two highest energy levels $4^2P_{1/2}$ and $4^2P_{3/2}$ on the P-orbital are presented in

Figure 2.4 (1). The $4^2S_{1/2} \longleftrightarrow 4^2P_{1/2}$ dipole transition at 397 nm can be used for state detection as well as Doppler cooling. However, there is a 7.5% probability for a valence electron to decay from $4^2P_{1/2}$ to $3^2D_{3/2}$ as this is a dipole allowed transition [13]. To counter this, 866 nm laser light is used for repumping the $3^2D_{3/2}$ state to the $4^2P_{1/2}$ state during cooling and detection of the ion. Another laser at 854 nm is used for repumping from $3^2D_{5/2}$ to $4^2P_{3/2}$ from where it swiftly decays to the $4^2S_{1/2}$ state.

Figure 2.4 (2) shows the Zeeman level splitting of D- and S-orbitals in the presence of a magnetic field B. In the absence of the magnetic field the transition frequency between the $4^2S_{1/2}$ and $3^2D_{5/2}$ states is denoted as ω_0. When the B field is applied the transition frequency is determined by the following equation [14], [15]

$$\omega_{(D,S)} = \frac{\mu_B}{h}\left(g_J(\mathrm{D}_{5/2})m^* - g_J(\mathrm{S}_{1/2})m\right)B, \tag{2.8}$$

where μ_B is Bohr magneton ($\mu_B/h = 1.399\,\mathrm{MHz/G}$), $g_J(\mathrm{S}_{1/2}) = 2.00225664(9)$ [16] and $g_J(\mathrm{D}_{5/2}) = 1.2003340(3)$ [17] are the Lande g-factors, m^* and m are the magnetic quantum numbers of $3^2D_{5/2}$ and $4^2S_{1/2}$ respectively. There are 10 electric quadrupole transitions, which are allowed by the following selection rules: $\Delta m = m_D - m_S = 0, \pm 1, \pm 2$

2.4 Interaction between a laser field and a quantum two-level system in a harmonic potential

In this section the interaction between laser light and the ion confined in the Paul trap will be considered. This interaction can be characterized by the Hamiltonian H:

$$H = H_{\mathrm{atom}} + H_{\mathrm{trap}} + H_{\mathrm{laser}}, \tag{2.9}$$

where $H_{\mathrm{atom}}, H_{\mathrm{trap}}, H_{\mathrm{laser}}$ will be considered separately.

The ion is described by two levels $|S\rangle$ ($4^2S_{1/2}$) and $|D\rangle$ ($3^2D_{5/2}$) with energy difference $\hbar\omega_0$; see Figure 2.4. The internal two-level system can be expressed in terms of Pauli spin matrices with Hamiltonian H_{atom} [18]:

$$H_{\mathrm{atom}} = \frac{\hbar\omega_0}{2}\sigma_z, \tag{2.10}$$

where σ_i is the Pauli spin matrix. Such a two-level system confined by a harmonic potential with oscillation frequency ω_z, and exhibits a motion that can be expressed in terms of annihilation (a) and creation ($a^\dagger$) operators with Hamiltonian H_{trap} [18]:

$$H_{\text{trap}} = \hbar\omega_z \left(a^\dagger a + 1/2\right). \tag{2.11}$$

The Hamiltonian H_{laser} describing the interaction between the laser field and a two-level quantum system is given by:

$$H_{\text{laser}} = \frac{\hbar\Omega}{2}\left(e^{i\eta(a^\dagger+a)}\sigma^+ e^{-i\omega_L t} + e^{-i\eta(a^\dagger+a)}\sigma^- e^{i\omega_L t}\right), \tag{2.12}$$

where ω_{L} is the laser frequency, $\sigma^\pm = (\sigma_x \pm \sigma_y)/2$ are electronic raising and lowering operators and Ω is the Rabi frequency, which determines the coupling strength between the two-level quantum system and the laser field. For a laser of wavelength λ, the so called Lamb-Dicke parameter η, is given by:

$$\eta = \frac{2\pi}{\lambda}\sqrt{\frac{\hbar}{2m\omega_z}}. \tag{2.13}$$

Let us assume that the two-level system is cooled into the Lamb-Dicke regime $\eta^2(2n+1) \ll 1$, where n is a motional quantum number [18]. In such a regime the wavelength of the laser field is much bigger than the size of the motional wavefunction of the ion. Therefore the coupling strength between $|D,n\rangle$ and $|S,n\rangle$ is given by:

$$\Omega_{n,n} = \Omega(1 - n\eta^2). \tag{2.14}$$

If the laser is detuned by a frequency $\pm\omega_z$ then transitions $|D,n\rangle \longleftrightarrow |S,n-1\rangle$ and $|D,n\rangle \longleftrightarrow |S,n+1\rangle$ will be induced, which are known as blue and red sidebands. Their coupling strength are

$$\Omega_{n,n+1} = \Omega\eta\sqrt{n+1}, \tag{2.15}$$

$$\Omega_{n,n-1} = \Omega\eta\sqrt{n}. \tag{2.16}$$

2.5 Cooling and detection of the ion

In order to use the ion as a two-level quantum system (qubit) for building a quantum computer, it has to be initialized in the ground state of motion (Figure 2.5). For this purpose Doppler cooling and sideband cooling have to be performed. The heating rate

measurement presented in section 3 also requires cooling as a necessary step. In addition, the transition between S and P-orbitals, which is used for Doppler cooling, allows us to image the ion and detect its state.

Detection

The measurements presented in this thesis rely on measuring the probability for finding the ion in the $|S\rangle$ and $|D\rangle$ states. The 397 nm light is scattered when the $4^2S_{1/2} \longleftrightarrow 4^2P_{1/2}$ transition is driven. In this way, the ion is in the $|S\rangle$ state if the 397 nm light was collected by a CCD camera and photomultiplier (PMT); see section 4. However the signal on the PMT or CCD is zero (no fluorescence is detected) when the ion is in the $|D\rangle$ state. This technique is called electron shelving [19] and allows one to detect the electronic state of the ion with an efficiency close to 100% [20].

Doppler cooling

When $\omega_z \ll \Gamma$, where Γ is the natural linewidth of the cooling transition, multiple photons can be emitted or absorbed during one oscillation of the trapped ion. Such a condition is called the weak binding regime [21]. In our case $\omega_z = 2\pi \times 1\,\mathrm{MHz}$ and $\Gamma/2\pi = 22.4\,\mathrm{MHz}$ such that this conditions is satisfied and the ion can be seen as a two-level atomic system ($4^2S_{1/2} \longleftrightarrow 4^2P_{1/2}$) with energy difference ω_{SP}. If the laser light with frequency ω_{L} is switched on and pointed at the ion, the excitation of the electronic state is induced. Hence the momentum of the ion increases by $\hbar\omega_L/c$ in the direction of the laser, where c is the speed of light. When the laser light is detuned to the red by $\Delta = \omega_L - \omega_{SP}$, due to the Doppler effect, the ion absorbs photons at a higher rate when moving in the direction opposite to the laser beam. Therefore, after a number of absorption and emission cycles, the ion velocity slows down.

For the optimal detuning $-\Delta/2$, Doppler cooling can reach a temperature minimum T_{min} and a minimum mean phonon number $\overline{n}_{min}$ which are given by [21]:

$$T_{\mathrm{min}} = \frac{\hbar\Delta}{2k_{\mathrm{B}}}, \tag{2.17}$$

$$\overline{n}_{\mathrm{min}} = \frac{T_{\mathrm{min}}k_B}{\hbar\omega_z} = \frac{\Delta}{2\omega_z}, \tag{2.18}$$

where k_B is the Boltzmann constant. In our system with an axial frequency $\omega_z = 2\pi \times 1\,\text{MHz}$, Lamb-Dicke parameter $\eta_{397} = 0.07$ and using equation (2.18) gives the Doppler limit of motional quanta $\bar{n}_{\text{min}} \sim 11$. Therefore, with Doppler cooling the Lamb-Dicke regime is reached, $\eta^2(2\bar{n}_{\text{min}} + 1) \ll 1$.

Sideband cooling

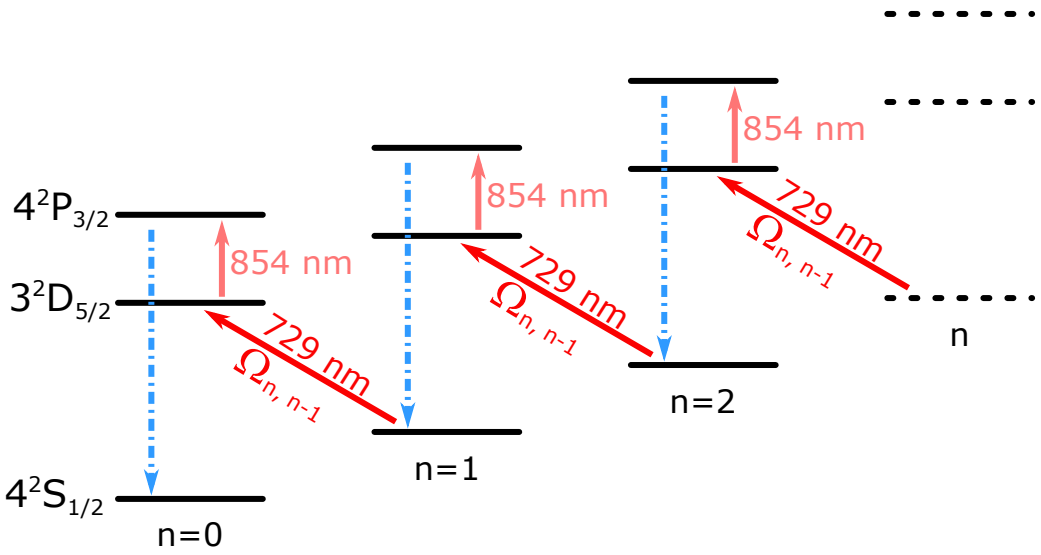


Figure 2.5: Sideband cooling scheme. The frequency of the 729 nm laser is red detuned in such way that the $|S,n\rangle$ state is coupled to the $|D,n-1\rangle$ state. Consequently, each time when the ion is pumped to the $3^2D_{5/2}$ state the motional quantum number is reduced by one until it reaches the state with $\bar{n} \approx 0$. The 854 nm laser light is used to pump the ion from $3^2D_{5/2}$ state to $4^2P_{3/2}$ state.

The sideband cooling scheme requires the Lamb-Dicke regime (see section 2.4) and addressing of frequency resolved sidebands. The criteria for frequency resolved sidebands are $\Delta_L \ll \omega_z$, where Δ_L is the linewidth of the 729 nm laser and $\omega_z \gg \Gamma$, where $\Gamma \approx 1\,\text{Hz}$ is the natural linewidth of the $4^2S_{1/2} \longleftrightarrow 3^2D_{5/2}$ transition. The sideband cooling scheme is depicted in Figure 2.5. The frequency of a 729 nm laser is red detuned ($\Delta = \omega_D - \omega_z$) in such way that the $|S,n\rangle$ state is coupled to the $|D,n-1\rangle$ state. Consequently each time when the ion is pumped to the $3^2D_{5/2}$ state the motional quantum numbers is reduced by one until it reaches the state with $n = 0$. At this point of time, the coupling strength on the red sideband reaches zero and the ion is cooled to the motional ground state. However, the

decay rate from $3^2D_{5/2}$ to $4^2S_{1/2}$ is very large 1.17 s. And in order to speed up the process the ion is pumped from $3^2D_{5/2}$ to $4^2P_{3/2}$ by means of 854 nm laser light, from where the ion swiftly (6.9 ns) decays to the $4^2S_{1/2}$ state with high probability [22].

CHAPTER 3

Motional heating in surface ion traps

The metastable exited state and the ground state of the ion are commonly used as a two-level quantum system (qubit), the motional common modes of the ions trapped in the harmonic oscillator can be used to perform quantum gate operations, for example a Mølmer-Sørensen gate [23]. An increase of phonons coupled from the environment during the gate execution reduces the fidelity of its operation [18]. The parameter which describes how fast the ion heats up from the ground state to the first excited state is called the motional heating rate. The motional heating is a crucial parameter for an ion trap and it should be measured and characterized [6].

Important sources of the heating rate in trapped ion experiments are technical noise, Johnson—Nyquist (Johnson) noise, and surface noise [6]. Technical noise can be caused by electronic devices like power supplies as well as electromagnetic interference from nearby electronics. Johnson noise is caused by thermal motion of charge carriers in conductors [24, 25]. Surface noise arises from different physical processes related to the trap surface material [6].

In chapter 5, we measure the frequency spectrum and temperature dependence of the electric-field noise to differentiate and characterize different noise sources. The aim of this chapter is to briefly outline theoretical aspects and measuring techniques of heating rates,

which are relevant for the experiments described in chapters 5 and 6. Some parts of this chapter are extracted from the article [26].

3.1 Motional heating rate of a trapped ion

In practical terms, electric-field noise couples to the ion and adds phonons to its motional state at a rate Γ_{h}. A distribution of the power into the frequency components of the electric-field noise is called electric-field spectral density and denoted by $S_E(\omega)$. The relation between the heating rate Γ_{h} and the electric-field noise spectral density $S_E(\omega)$ at the position of the ion is [6]

$$\Gamma_{\mathrm{h}} = \frac{q^2}{4m\hbar\omega} S_E(\omega), \tag{3.1}$$

with $\hbar$ the reduced Planck constant, q and m the ion's charge and mass, and ω its motional frequency. The electric-field spectral density can arise from different noise sources. The study of this term is used to identify the noise source of the heating rate because S_E depends on many measurable variables such as frequency, temperature, ion-electrode separation, *etc*.

3.2 Sources of heating in surface ion traps

The origin of the heating rate could be associated with many noise sources and some of them are still unknown [6]. The most common are Johnson—Nyquist noise, different noise sources related to the trap surface, technical noise, noise sources related with the electromagnetic environment and the RF pick up [6]. In this section the noise sources which are relevant for this thesis will be described.

Johnson—Nyquist noise

Let us consider an ideal resistor with a resistance R in a thermal bath at constant temperature (T); see Figure 3.1. An electromotive force ε of the thermal noise appears across the resistor. It arises from the chaotic (thermal) movement of charge carriers inside of the resistor. For a given frequency ω this voltage noise has the following spectral density [25, 24]:

$$S_V = 4k_{\mathrm{B}}TR(\omega, T), \tag{3.2}$$

where k_B is Boltzmann's constant, T the temperature of the resistor causing the noise and R the resistance. This model considers an ideal resistor which generates thermal white noise whose spectral components are uniformly distributed over the entire range of frequencies. The related electric-field noise at the position of the ion is given by the equation:

$$S_E = \frac{S_V}{\delta_c^2}, \tag{3.3}$$

where δ_c is a geometry-dependent characteristic distance [6]. Essentially, for a given electrode j with applied voltage V_j and the electric-field E_i^j the characteristic distance is $\delta_{i,j} = \frac{V_j}{E_i^j}$. Detailed information on how to calculate δ_c for trap electrodes in chapter 5 is given in [27].

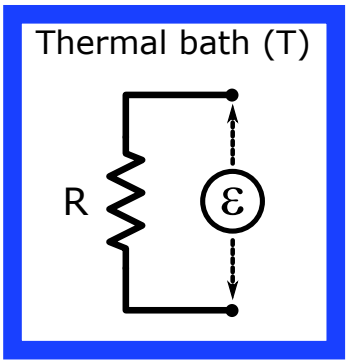


Figure 3.1: Model of an ideal resistor in a thermal bath. Thermal excitations induce a fluctuating voltage across the resistor.

This model considers an ideal resistor which generates thermal white noise.

Two-level fluctuator models

The close proximity of the ion to the electrodes of the trap leads to high sensitivity to noise sources that originate from the surface of the trap. The surface roughness and surface defects create dislocations in the solid's lattice. This leads to the formation of local minima in the periodic structure of the surface. The electron, atom or the group of atoms can be confined in these minima [28]. Therefore, random jumps from one minimum to another can occur due to thermal activation or quantum tunneling through the barrier. The outcome of such a process is fluctuations of the local dipole moment. In fact, the localized charges

in the solid's lattice can be considered as a specific class of two-level fluctuators (TLFs) [6].

It is possible to explain a wide variety of effects in solids by means of TLFs. For example, because of the presence of TLFs, the specific heat of glasses at low temperatures follows a linear temperature dependence [29]. Large amount of such TLFs with wide range of energy barriers can be found in amorphous materials and typical solids. In superconducting qubits, it has been possible to investigate and address two-level fluctuators individually [30]. Another example of the role of TLFs on physical properties of solids is anomalous charge noise in single-electron transistors and quantum dots [31, 32, 33]. In the case of surface ion traps, TLFs may explain the anomalous heating which is one of the limitations for large-scale quantum computers [6]. TLFs can be localized in any insulating layer on top of the electrodes, even if they are made from noble metals, causing noise which leads to the heating of the ion.

The microscopic picture of the noise induced by excitations of TLFs which is affecting the ion confined above the metallic surface can be described in terms of dipoles located on the surface. These dipoles generate electric-field fluctuations giving rise to the heating of motional states of the ion. In practical terms, TLF models consider the double-well potential in which real or effective particles undergoing random transitions between two quantum states. These quantum states are separated by an energy barrier and have different electric dipole moments. Transitions between the TLF states at a rate ω_0 induced by thermal activation lead to electric-field fluctuations with a spectral density [6]

$$S_E^{(\mathrm{TLF})}(\omega) = A\frac{\omega_0}{\omega_0^2+\omega^2}, \tag{3.4}$$

where $A(T) = A_0 \cosh^{-2}(T_0/2T)$, $k_B T_0$ is the activation energy of the fluctuator and A_0 is prefactor which is proportional to the dipole moment of the charged particle [28]. If one considers a uniform distribution of energy difference between two wells of potential over the relevant frequency range, the following dependence for the full range of temperatures takes place $S_E^{(\mathrm{TLF})}(\omega,T) \sim T/\omega$ [6]. In our experiment, see chapter 5, the noise level was estimated to be $S_E \approx 1\times 10^{-14}\,\mathrm{V^2 m^{-2} Hz^{-1}}$ at frequency $\omega = 2\pi\times 1\,\mathrm{MHz}$ and an electrode ion separation of $230\,\mu\mathrm{m}$ [6]. This value is considered to be small but measurable with trapped ions if the other noise sources are suppressed.

3.3 Heating rate measurement

There exist several techniques to measure the heating rate. A first method is laser recooling. It relies on the fact that the fluorescence of the ion is influenced by its motion when the ion is Doppler cooled [34]. A second method is similar to the recooling method but instead of measuring the time dependence of the fluorescence, time-resolved ion images in the axial direction are collected after the variable heating time. This allows accessing the temperature of the ion from the average oscillation amplitude [35]. A third method is to measure the escape rate of the ion from the trap while all cooling is turned off [36]. The above methods are useful for measuring relatively high heating rates, $\Gamma_{\mathrm{h}} \gg 1000$ phonons/s, and are not optimal for our experiments. The method of choice consists of measuring the excitation of resolved sidebands to access the heating rate [18]. The motional heating rate is accessed from the ratio of the excitation probabilities of the blue and red sidebands, measured as a function of the time delay after the excitation pulse. With this method, one can detect differences in phonon numbers below 0.1 phonons. In all experiments described in this thesis, the sideband method is used because of its simplicity and robustness.

In order to measure the heating rate with the sideband method, the ion should be prepared in the ground state of its axial mode by Doppler cooling, followed by sideband cooling, see section 2.5. A narrow linewidth 729 nm laser tuned to the $S_{1/2} \leftrightarrow D_{5/2}$ quadrupole transition is successively switched between red and blue sidebands. After this step the electronic state of the ion is measured with the shelving technique, see section 2.5. The full sequence of laser pulses required for the experiment is shown in Figure 3.2. It includes Doppler cooling, optical pumping, sideband cooling, blue/red sideband pulse, detection and repumping. Note that the sideband cooling section consists of several successive pulses of cooling and optical pumping. Usually for optimal ground state cooling, 7 to 10 sideband cooling repetitions are necessary.

The motional state of the ion can be described by the thermal distribution. The probability to find an ion in the nth motional state is [18]

$$P_n = \frac{\overline{n}^n}{(1+\overline{n})^{n+1}}, \tag{3.5}$$

where $\overline{n}$ is an average phonon number. When applying a pulse on resonance with the red or blue sideband, the probability to measure the ion in the excited state $|D\rangle$ after a waiting time t (Figure 3.2) is given by

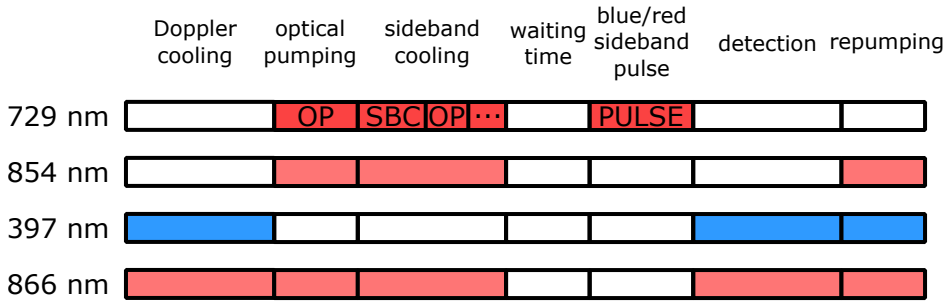


Figure 3.2: The full sequence of the laser pulses required for a heating rate measurement.

$$
\begin{aligned}
P_{|D\rangle}^{RSB}(t) &= \sum_{n=1}^{\infty} P_n \sin^2\left(\frac{\Omega_{n,n-1}t}{2}\right), \\
P_{|D\rangle}^{BSB}(t) &= \sum_{n=0}^{\infty} P_n \sin^2\left(\frac{\Omega_{n,n+1}t}{2}\right),
\end{aligned}
\tag{3.6}
$$

where $\Omega_{n,n-1}$ and $\Omega_{n,n+1}$ are the coupling rates of the blue and red sidebands. By combining equations (3.5, 3.6) and taking into consideration $\Omega_{n,n+1} = \Omega_{n+1,n}$, we can derive the following [18]:

$$
\begin{aligned}
P_{|D\rangle}^{RSB}(t) &= \sum_{n=1}^{\infty} \frac{\bar{n}^n}{(1+\bar{n})^{n+1}} \sin^2\left(\frac{\Omega_{n,n-1}t}{2}\right) \\
&= \frac{\bar{n}}{(1+\bar{n})} \sum_{n=1}^{\infty} \frac{\bar{n}^n}{(1+\bar{n})^n} \frac{1}{1+\bar{n}} \sin^2\left(\frac{\Omega_{n,n+1}t}{2}\right) \\
&= \frac{\bar{n}}{(1+\bar{n})} P_{|D\rangle}^{BSB}(t)
\end{aligned}
\tag{3.7}
$$

Rewriting equation 3.7 yields the mean phonon number

$$
\bar{n} = \frac{P_{|D\rangle}^{RSB}}{P_{|D\rangle}^{BSB} - P_{|D\rangle}^{RSB}}. \tag{3.8}
$$

Note that this equation does not depend on pulse length, Rabi frequency or Lamb-Dicke parameter. Therefore the motional heating rate of the ion can be measured by probing of blue and red sidebands for different waiting times after ground state cooling; see Figure 3.2.

CHAPTER 4

Experimental setup

In this chapter we give the basic information about the experimental setup used to obtain the results in chapters 5, 6, 8 is given in this chapter. The setup was built by Michael Niedermayer and described in detail in his PhD thesis [9]. The experimental setup was constructed to fulfill the following requirements:

1. Possibility to mount different trap designs
2. Adaptable to cryo-electronics
3. Low level of technical noise
4. Low level of mechanical vibrations
5. Access to the trap chip for multiple laser beams
6. Fast trap chip exchange

The core element of the experimental setup is the trap chip which can vary depending on the research objective. In this thesis, several different trap types have been used: silicon based surface ion traps (see section 6.3), a trap chip made of a high-temperature

superconductor (see section 5.2) and the surface ion trap from Seoul National University (SNU) (see section 8.1). Each of these traps requires modifications of the trap carrier and the electrical circuit of the trap setup in order to be operable.

4.1 Cryogenic apparatus

Gifford-McMahon refrigeration cycle

We use a two-stage Advanced Research Systems ARS-10HW cryostat (Figure 4.1) with a pneumatically driven Gifford-McMahon (GM) refrigeration cycle [37]. The fluid expansion refrigeration method and apparatus were developed by William E. Gifford and Howard O. McMahon in 1959 [37]. Pneumatically driven cryostat means that the cryo cycle uses the internal pressure difference to move the displacer; see 4.1 (a). Pneumatically driven cryostat consists of less amount of the moving parts inside of the coldhead and hence minimizes vibrations of the setup [38].

In general, the GM cryostat consists of a coldhead, compressor, vacuum shroud and the radiation shield. The coldhead contains the displacer, regenerating material and the motor. The coldhead is connected to the compressor via two helium gas lines. The first line supplies high pressure (HP) gas to the coldhead, while the second one returns low pressure (LP) gas from the coldhead; see 4.1 (a). The compressor is used to supply the coldhead with the pressurized helium gas, as well as clean the gas with a filter (adsorber) during the cooling cycle. The vacuum shroud surrounds the cold end of the coldhead in order to minimize thermal losses via conduction and convection. The radiation shield is cooled by the 50K stage of the coldhead and insulates the 4K stage from room temperature thermal radiation [39].

The refrigeration cycle of the GM cooler consists of four steps which are listed below:

1. The motor in the coldhead switches the valve to open the high pressure path; see 4.1 (a). This step allows high pressure helium gas to move trough the regenerating material into the expansion area.

2. The created pressure difference shifts the displacer upwards. The helium gas at the bottom of the coldhead expands and cools down.

3. The motor in the coldhead switches the valve to open the low pressure path; see

4.1 (a). Hence, cold helium gas flows through the regenerating material which extracts the heat from the system.

4. The displacer returns to its initial position because of the pressure difference. The cycle is completed.

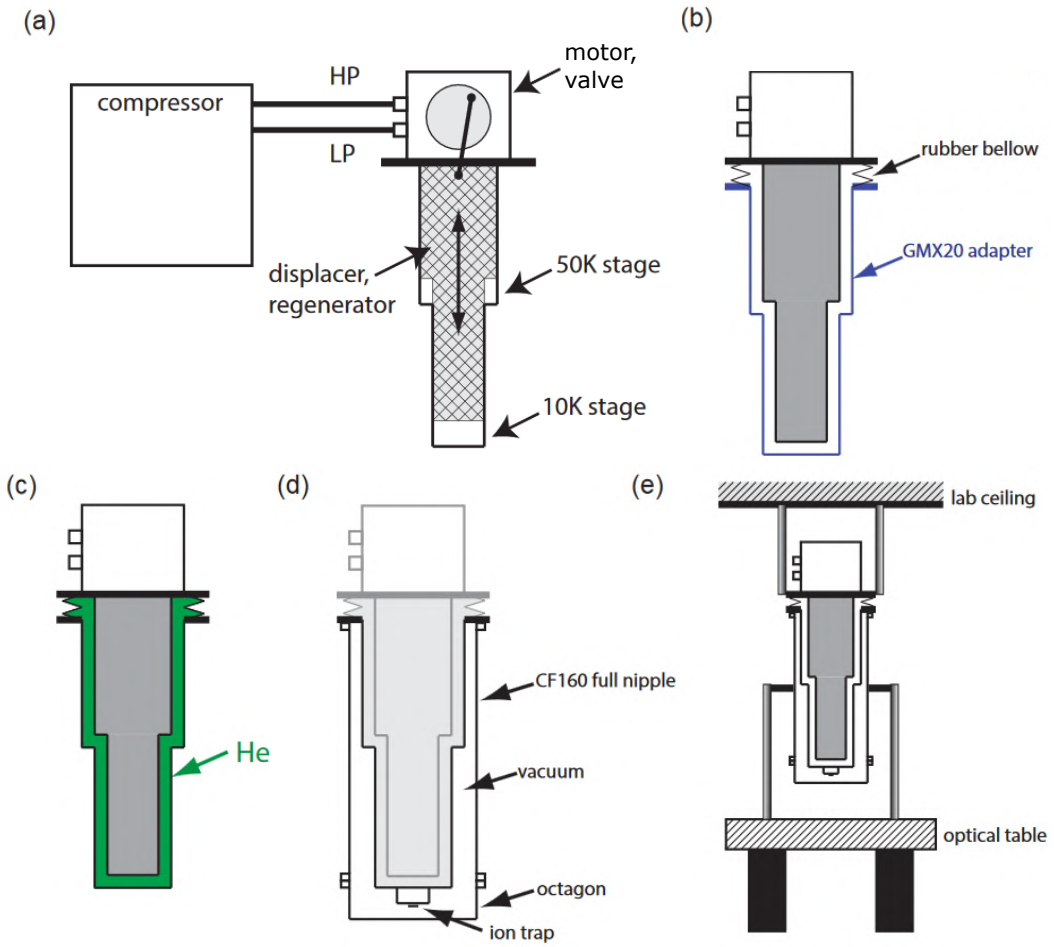


Figure 4.1: (a) Cross-section of the coldhead. Motor and displacer are the moving during the cryogenic cycle, causing horizontal and vertical vibrations. (b) Coldhead with attached rubber bellow and adapter (GMX20). (c) The volume between adapter and coldhead is filled with helium gas. (d) CF160 nipple and octagon form the vacuum chamber, in which the trap chip is placed. (e) The coldhead is connected to the laboratory ceiling and the vacuum chamber is located on the optical table. Figure courtesy of Michael Niedermayr [9]

The above described GM refrigeration cycle ensures that the sample can be cooled

down and warmed up in a period of 12 hours, which is short compared to other systems [38]. This fulfills point 6 of our general setup requirements.

Vibration isolation

Gifford-McMahon cryostats have one significant drawback, namely a high level of vibration caused by moving parts (motor, displacer) inside of the coldhead (Figure 4.1 (a)). The typical vibration level in the horizontal plane of the surface ion trap of the GM cryostat is $\sim 20\,\mu m$ [38]. For comparison, in our experimental setup the 729 nm laser with $30\,\mu m$ beam width is used to address the qubit transition; see section 4.4. The ion would move with respect to the addressing laser beam, such that the beam intensity experienced by the ion fluctuates. Therefore, the fidelity of quantum gates can degrade [40]. For this reason, vibration isolation of the cryostat is an important requirement that must be satisfied by the experimental setup.

We use a helium buffer gas to thermally couple the coldhead to the trap without inducing significant mechanical vibration. This method provides good thermal conductivity which allows the trap chip to be cooled down to temperatures of less then 10 K. The ARS GMX20 adapter and the rubber bellow (Figure 4.1 (b)) are used to create a volume between the coldhead and the vacuum chamber which is filled with helium buffer gas (Figure 4.1 (c)). The vacuum chamber consists of a CF160 nipple and the octagon, depicted in the Figure 4.1 (d). The trap chip is mounted in the middle of the octagon. The coldhead is attached to the laboratory ceiling and the vacuum chamber is located on the floating optical table (Figure 4.1 (e)). Hence the vacuum chamber is mechanically decoupled from the coldhead by means of a rubber bellow and thermally coupled to the coldhead via helium gas.

The vibrations of the resulting setup were measured with a laser interferometer (SIOS SP 2000 DI) and a mirror attached to one of the windows of the octagon. The axial vibrations of the vacuum chamber have been reduced down to the $200 - 300\,nm$ level and radially down to $\sim 190\,nm$. Compared to our typical laser beam with a waist of $30\,\mu m$ such vibrations would cause intensity fluctuations of less than 1%, small enough for the measurements presented in this thesis.

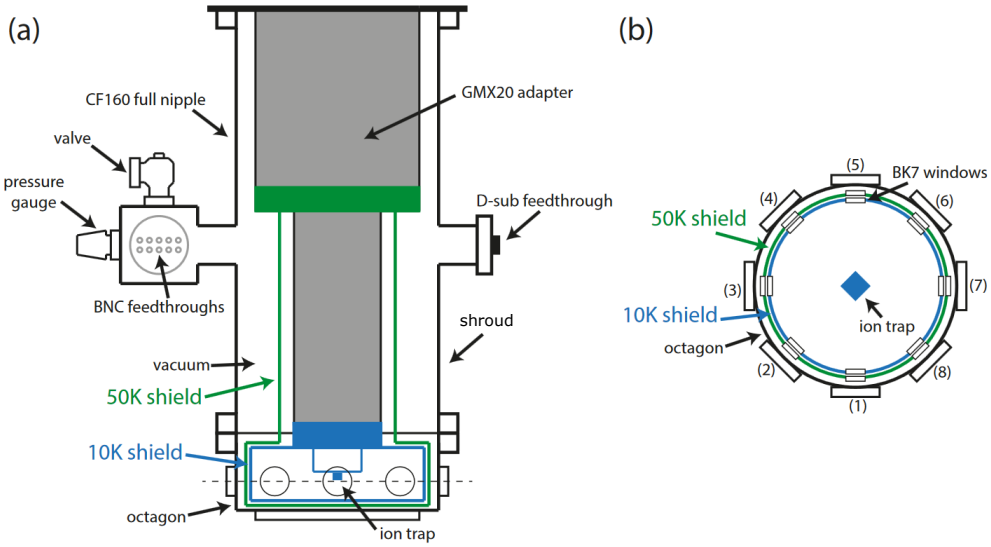


Figure 4.2: (a) Cross-section of the cryostat. The vacuum shroud is mounted on the GMX20 adapter. It consists of a CF160 full nipple and the CF160 octagon. The trap chip is mounted in the 10 K shield inside of the octagon. D-sub feedthroughs are used to connect heaters and temperature sensors. BNC feedthroughs are used to supply the ion trap with RF and DC signals. (b) Cross-section of the CF160 octagon. Seven viewports (1, 3-8) are used for laser access and one viewport (2) is used as an input for a neutral beam flux from a calcium oven. The bottom CF160 flange provides optical access for fluorescence detection. Figure courtesy of Michael Niedermayr [9]

4.2 Vacuum chamber

In this section, the vacuum chamber and related infrastructure will be discussed. The vacuum shroud is fastened to a GMX20 adapter; see Figure 4.2 (a). It consists of a homemade CF160 full nipple and a CF160 octagon vacuum chamber, mounted on a floating optical table. The CF160 full nipple contains the vacuum valve, pressure gauge, BNC feedthroughs and D-sub feedthroughs. A vacuum pump is attached to a valve, and is used to evacuate the octagon. A pressure gauge is used to monitor the vacuum pressure. BNC feedthroughs and steel coax cables which are thermally anchored are used to connect the trap chip with DC and RF power supplies. On the side of the vacuum shroud D-sub feedthroughs are used to connect thermal sensors and heaters with the cryogenic control system Cryo-con 24 [a].

[a] Model 24 Cryogenic Temperature Controller

The CF160 octagon consists of eight CF40 flanges and one CF160 bottom flange; see Figure 4.2 (b). The CF40 flange, labeled (2) (Figure 4.2 (b)) is connected to a small vacuum chamber with a calcium oven. The other seven flanges (labeled (1), (3-8)) contain BK7 viewports for laser beam access. Flanges (1), (3), (5) and (7) support four magnetic coils with 90 mm diameter. These coils are used in Helmholtz configuration and each of them are made out of 248 copper windings. The magnetic field produced b the coils defines the quantization axis for the ion and split the otherwise degenerate Zeeman sublevels.

The ionic fluorescence is collected through the bottom CF160 flange. It is broadband anti-reflection coated, providing optical transmission of more than 99.5% at 397 nm.

4.3 Trap setup

In the following section, an overview of the in-cryo trap setup will be presented. It consists of a copper carrier to which the trap chip is attached; see Figure 4.3 (2). The DC filters (see section 4.3) and the RF resonator (see section 4.3) are glued to the trap carrier; see Figure 4.3 (1). The temperature sensor is located ~ 3 cm far from the trap chip and attached to the H-shaped copper carrier with a brass screw.

RF resonator

The RF voltage is generated by a function generator placed outside of the cryostat and is stepped up by an LC resonator placed next to the trap chip inside of the cryostat; see Figure 4.4 (2). Such a scheme allows us to apply high RF (up to 100 V) voltage to the trap with minimum heat load on the H-shaped copper carrier, thus achieving a low trap chip temperature (~ 15 K). The LC resonator is built out of a homemade copper coil with impedance L_2 and capacitance of the trap chip C_{trap} (Figure 4.4 (2)). The frequency of this resonator is given by the formula:

$$f_0 = \frac{1}{2\pi\sqrt{L_2 C_{\text{trap}}}}. \tag{4.1}$$

We characterize the resonator with the quality factor Q which is proportional to the voltage gain(see section 6.4):

$$Q = \frac{2\pi f_0 L_2}{R_1} = \frac{1}{R_1}\sqrt{\frac{L_2}{C_{\text{trap}}}} = \sqrt{\frac{Z}{R_1}}G, \tag{4.2}$$

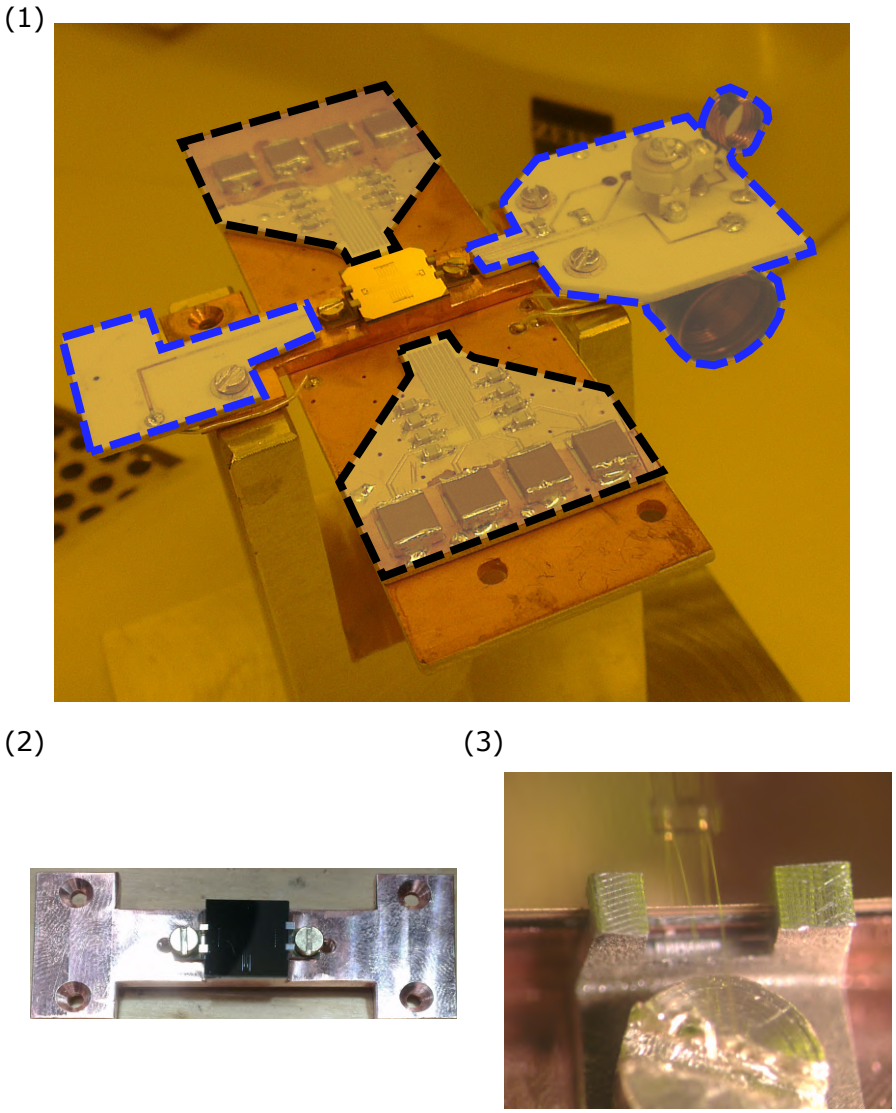


Figure 4.3: (1) The picture of the trap setup with the trap chip, RF resonator (marked by the dashed blue lines), DC filters (marked by the dashed black lines). The temperature sensor is located on the H-shaped copper carrier. (2) H-shaped copper carrier with attached trap chip. (3) Fork-shaped titanium clamps which are used to mount the trap chip to the copper carrier.

where G is the voltage gain, Z is the impedance of the circuit and R_1 is the resistance of the coil.

In order to minimize reflections in the RF circuit, a matching network is utilized. It matches the impedance of the LC resonator with cables to the impedance of the function generator. It consists of a homemade coil L_1 and an adjustable capacitor $C_{\text{adj.}}$; see

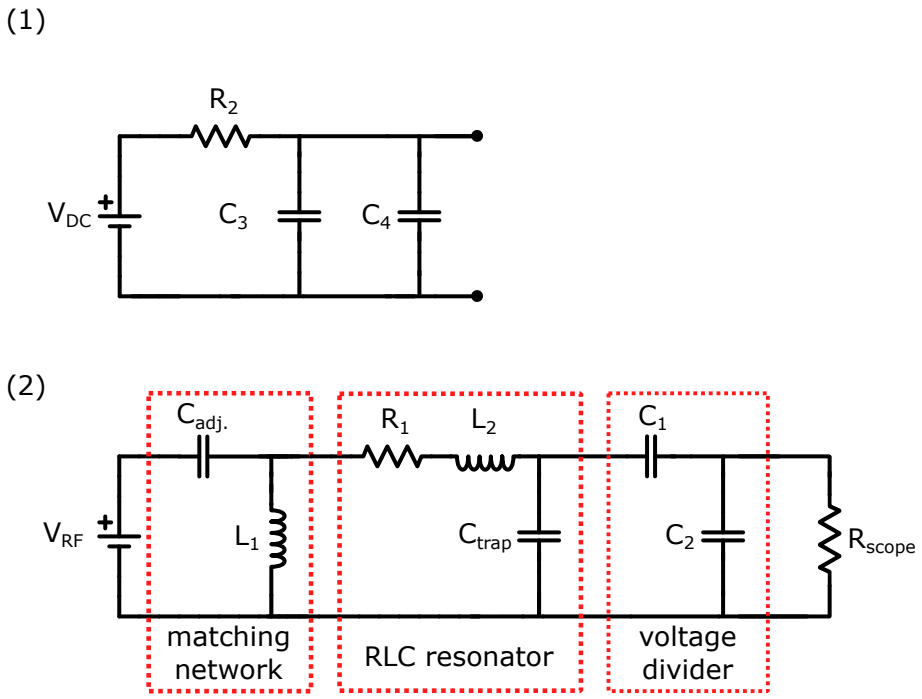


Figure 4.4: (1) Low pass filters ($C_3 = 300\,\text{nF}$, $C_4 = 470\,\text{pF}$ and $R_2 = 100\,\Omega$) with cut-off frequency 4.8 kHz are attached to all DC electrodes of the trap chip. (2) An RF resonator is used to supply the trap chip with an RF signal. It consists of a frequency generator, a matching network ($C_{\text{adj.}} = 12 - 100\,\text{pF}$ and $L_1 = 168\,\mu\text{H}$), an LC resonator (R_1, $L_2 = 6.3\,\mu\text{H}$, $C_{\text{trap}} \sim 10 - 20\,\text{pF}$), a voltage divider ($C_1 = 2.4\,\text{pF}$ and $C_2 = 1000\,\text{pF}$) and an oscilloscope.

Figure 4.4 (2).

Another important part of the RF circuit is the voltage divider. It is used to directly sample the voltage V_{VD} on the trap chip while increasing the capacitance of the LC resonator only minimally. It consist of two capacitors C_1 and C_2 (Figure 4.4 (2)) placed in series between the LC circuit and ground. With an oscilloscope we measure the signal between the capacitors, at a reduced voltage given by:

$$V_{\text{VD}} = V_{\text{RF}} \frac{C_1}{C_1 + C_2}. \tag{4.3}$$

DC filters

It is important to ensure that the ions trapped by surface ion traps do not experience electrical noise coming from the DC lines. Therefore, it is important to filter the DC lines

in the frequency range of the desired motional frequencies. For that we use first-order low-pass RC filters (C_3, C_4 and R_2); shown in Figure 4.4 (1). We used components which are cryogenically compatible such as thin-film resistors [b] and NP0 capacitors [c]. We also ensure that all DC electrodes are efficiently grounded at RF frequencies to suppress RF pick-up. Therefore, the capacitor C_4 (Figure 4.4) is placed as close as possible ($\sim 1\,\text{cm}$) to the DC electrode. The resulting cut-off frequency of the low-pass filters is 4.8 kHz, which is orders of magnitude lower than typical trapping frequencies of $\sim 0.5 - 4\,\text{MHz}$.

Trap mounting of the Silicon ion traps

One of the challenges was mounting silicon based surface ion traps on the H-shaped copper carrier; see Figure 4.3 (2). There have been several attempts to glue the trap chip to the copper. However, all of them failed liquid nitrogen dipping tests (the trap was detached from the H-shaped copper carrier). We conclude that because of the different thermal expansion coefficients of copper and silicon, it is not possible to use glue in cryogenic environment. A solution for this issue is presented in Figure 6.17 (1). Titanium fork-shaped clamps are screwed to the copper carrier and fasten the trap chip. The titanium clamps act like a spring, and compensate for any thermal expansion shifts at cryogenic temperatures. The fork shape of the clamp is used to minimize the wire bonding length for RF and central DC electrodes. Another advantage of this mounting procedure is that one can mount or remove the trap chip from the copper carrier without using solvents.

4.4 Optical setup

In the following section, an overview of the laser setup and the ion detection setup will be presented.

In order to manipulate the $^{40}Ca^{+}$ ion we need to address it with four different lasers. A typical setup operation procedure starts with the ionization of neutral calcium atoms using 377 nm and 422 nm lasers. Doppler cooling and ion detection is performed with a 397 nm laser and is aided by a 866 nm repump laser. In order to perform sideband cooling of the axial motional modes, state detection and coherent operations the $4^2S_{1/2} \longleftrightarrow 3^2D_{5/2}$

[b] VPG, Y1625100R000Q9
[c] Kemet, C0805C471J1GACTU30Kemet and C2220C334J1GACTU

quadrupole transition has to be addressed with a 729 nm laser and repumped with a 854 nm laser from $3^2D_{5/2}$ to $4^2P_{3/2}$.

Photoionization of neutral calcium

In order to remove one electron from the calcium atom we use a two-step photoionization process; see Figure 4.5. A 422 nm laser is used to excite the transition $^1S_0 \longrightarrow {}^1P_1$. A 844 nm laser diode is frequency doubled to 422 nm with a homemade doubling cavity [41]. The 377 nm laser light, which is generated by a free running laser diode, is used for the transition from $^1P_1$ to the continuum. The individual lasers are focused with lenses and combined together with a bandpass filter FF01-377/50-25 (combiner 3 in Figure 4.6). Further information about photoionization can be found in the master's thesis of R. Lechner [41].

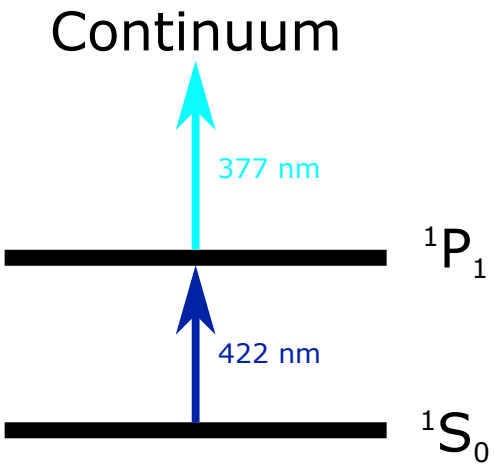


Figure 4.5: Two-step photoionization process with the calcium atom.

Doppler cooling and detection of the $^{40}Ca^+$ ion

The transition between the lowest energy level $4^2S_{1/2}$ and the $4^2P_{1/2}$ state is used to Doppler-cool the ion and detect the ionic fluorescence [42]. This transition is induced by laser light at a wavelength of 397 nm. Because of the dipole-allowed decay from $4^2P_{1/2}$ to the metastable $3^2D_{3/2}$ with a probability of roughly 1 per 17 decays [13], a laser with a wavelength of 866 nm has to be applied in order to pump back the population from $3^2D_{3/2}$

[13]. After Doppler cooling, a mean vibrational number of $\overline{n} \sim 10$ is achieved and further techniques are required to cool the ion down to the ground state.

A frequency-doubling system (Toptica,TA-SHG pro) produces the 397 nm laser light. The 866 nm laser light is generated with a diode laser (Toptica, DL100). Each of the laser is locked to a Fabry-Perot stabilization cavity with the Pound-Drever-Hall locking method [43]. The lengths of the cavities can be changed with piezoelectric actuators to adjust the lock ingredients frequency without changing their power. The 397 nm and 866 nm lights are sent to the experimental table via polarization-maintaining single-mode fibers. An AOM (Brimrose, QZF-80-20-397 with center frequency of 80 MHz) is used to switch on and off 397 nm laser light as well as to tune the laser power which is going to the ion. The same technique, but with a different AOM (Crystal Technology, AOM 3200-124 with center frequency of 200 MHz) is used for the 866 nm laser light. Then both 397 nm and 866 nm laser lights are sent via fibers to the laser combining optical setup; see Figure 4.6.

The FF01-395/11-25 (combiner 2 in Figure 4.6) is used to combine the photoionization beams with the 397 nm laser beam. In the laser combining optical setup, the 397 nm and the 866 nm beams are combined together with BLP01-595R-25 (combiner 1 in Figure 4.6). In order to focus and precisely manipulate overlapped beams (866 nm, 854 nm (see section 4.4), 422 nm, 397 nm, 377 nm) a single lens on a translation stage (xyz-stage (2)) is used; see Figure 4.6. After we load an ion we switch the path of 397 nm laser light to a second one (path 2), depicted in top of Figure 4.6, with a flip mirror in order to individually control the position of the 866 nm and the 397 nm beams.

Below the octagon, a custom made objective (focal length of 58 mm and NA $= 0.1$) is used to collect the 397 nm fluorescence light. The objective is mounted on an xyz-translation stage for precise alignment. The collected light is split by a 50/50 beamsplitter (Thorlabs, BSW20). One part of the light goes to a CCD camera (Andor, iXon+ A-DU897-DCS-BBB) and the second part goes to a photomultiplier (PMT, Hamamatsu, H7360-02).

Quadrupole transition

The 729 nm laser light is provided by the Quantum Information Processing laboratory at a Innsbruck University (located on the ground flour of the building) and transmitted via a 200 m polarization-maintaining single-mode fiber to our laboratory (located in the same building but on the fourth flour). The light in the CryoTrap laboratory is amplified by a

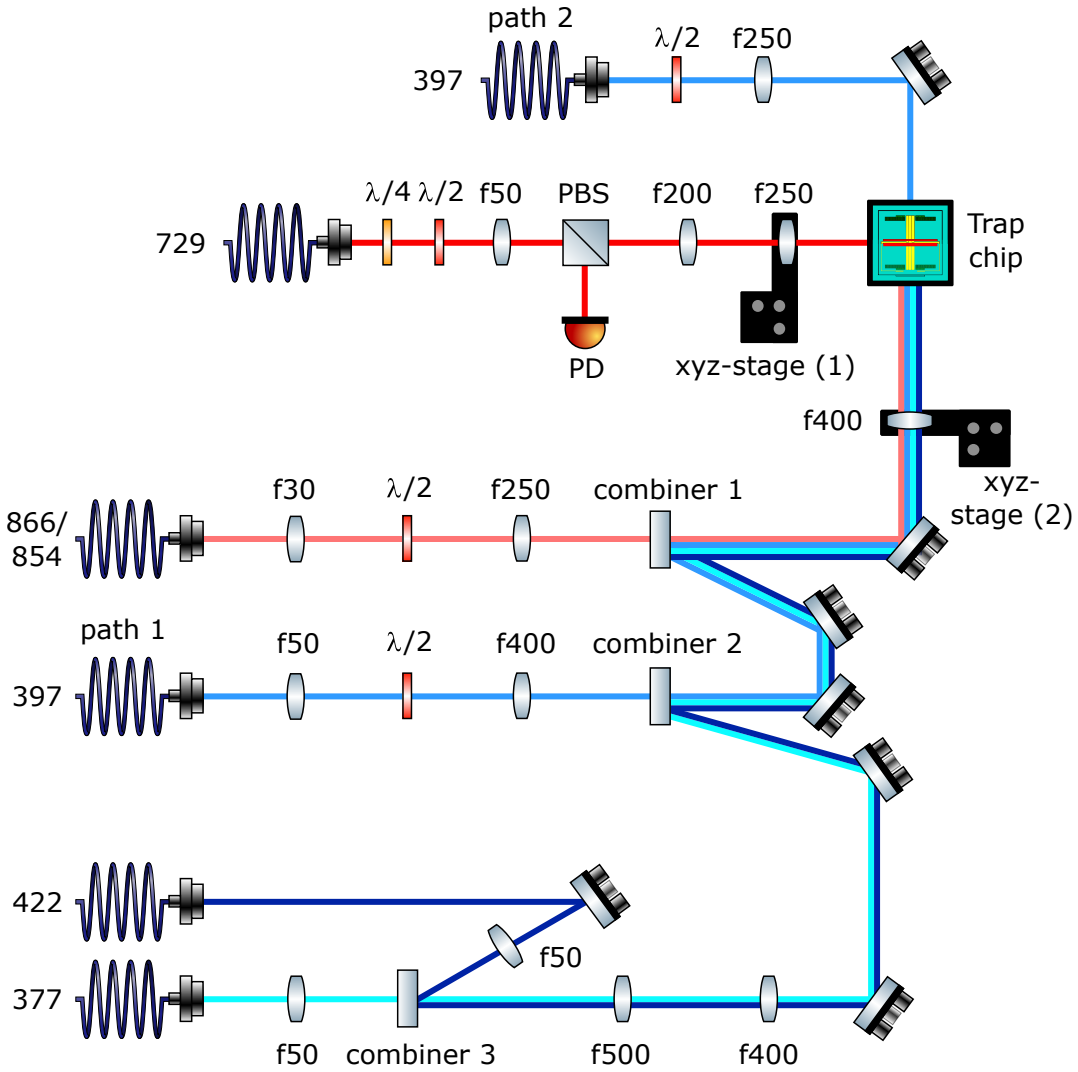


Figure 4.6: The laser combining optical setup. The 866 nm, 854 nm , 422 nm, 397 nm, 377 nm laser beams are combined and aligned together by using combiners 1,2 and 3 and mirrors. We use two optical paths for 397 nm laser light which are switchable with a flip mirror. One way (path 1) is dedicated for trapping an ion and the second way (path 2) is implemented for precise alignment of the Doppler beams. The 729 nm laser light is coupled from another side of the octagon.

tapered amplifier (Toptica, TA-100) and sent to the experimental table where it is controlled by an AOM (Crystal Technologies, 3270-122 with center frequency of 270 MHz). The beam is aligned to the trap chip with the setup labeled 729 in Figure 4.6. The intensity of the 729 nm laser light is monitored by a Si free-space amplified photodetector (Thorlabs

PDA36A-EC), labeled PD on the Figure 4.6. The intensity is controlled by an AOM (Crystal Technologies, 3080-122 with center frequency of 80 MHz).

An 854 nm laser light (Toptica, DL100) is used to pump the population from $3^2D_{5/2}$ to $4^2P_{3/2}$ states from where it decays to the $4^2S_{1/2}$ state. The 854 nm beam is combined with the laser path of the 866 nm beam.

4.5 Experimental control

The control of the experimental setup is done by two computers. This section describes the general functions of these computers.

PC1: temperature and pressure log; CCD camera control

The first PC is dedicated to CCD camera control, cryogenic system control and readout of pressure gauges.

We use Andor's SOLIS software to operate the CCD camera. The CCD camera is used for laser and objective alignment as well as for detecting neutral flux fluorescence. For temperature and pressure logging we use a homemade LabView program which was originally developed by Michael Niedermayr [44] and later modified to suit new experimental needs. We can measure temperatures at various places in the setup, using temperature sensors (LakeShore DT-670C-SD diode). A resistive heater can be accessed via Cryo-con 24 to heat up the 4 K stage. The LabView software collects information from two pressure gauges (Pfeiffer, PKR 251), one of which is connected to the vacuum pump station and the second one to the cryostat (Figure 4.2).

PC2: RF and DC signals; PMT; laser control

The second PC is used to control DC and RF signals, log PMT counts and laser controllers. On this PC we use a homemade LabView program called QFP 2.0. QFP 2.0 was written by Timo Körber (former member of the group) and was designed to control trapped ion experiments and collect experimental data. This software controls two analog output cards (National Instruments, PCI-6733 and PCI-6711). First card is used to control the voltage outputs for AOMs of 854 nm, 866 nm and 397 nm. Second card is used to collect the PMT data.

For producing laser pulses at well-controlled times, a pulse sequencer box [45] has been employed. This box generates transistor−transistor logic (TTL) signals, which are used to switch on and off AOM drivers for the 854 nm, 866 nm and 397 nm beams. This box also generates continuous RF signals, as well as RF pulses which directly control the AOM of the 729 nm beam.

The function generator (Marconi instruments 2024), which is used to produce the RF voltage on the trap electrodes, is also controlled with QFP 2.0. An additional LabView software has been written to control low-noise DC voltage source (ISEG, EHS F205x-F-K1) to supply DC trap electrodes.

CHAPTER 5

High-temperature superconducting ion traps

Electric field noise provides insights into microscopic processes, and imposes limitations to experimental systems. In particular, electric field noise in close proximity to surfaces creates obstacles for near-field measurements [46, 47], experiments with nitrogen-vacancy centers [48], Casimir effect studies [49], gravitational-wave detectors [50], and ion trapping experiments [6]. It has been suggested to employ the high sensitivity of trapped ions to electric field noise as a new tool in surface science [51]. In surface ion traps the closeness of the ions to the trap's electrodes leads to an increase of the electric field noise which directly leads to the higher heating rate of the motional state. The origin of this electric field noise is not well understood [6]. Trapped ions have been used to study the dependence of electric field noise on frequency, trap temperature and ion-surface distance [52, 53, 54, 55, 56, 35, 57] and have been combined with the analysis and removal of surface contaminants [58, 59, 57]. Recent studies [56, 35] indicate a d^{-4} scaling of the heating with the electrode-ion separation. Such scaling indicates that the origin of the electric noise originates from independent microscopic regions which are fluctuating on the surface of the electrodes. In this work, we use a surface-electrode ion trap containing

a high-temperature superconductor to investigate such surface noise source. In addition, we can study with an ion as probe the bulk material properties of the high-temperature superconductor.

To compare different sources of electric field noise in situ with a single device, we operate a surface ion trap made of YBCO, a high-temperature superconducting material. Design and simulations of the trap chip were done by Dominic Schärtl, additional details are presented in [27]. The trap works in two distinct regimes, above and below the critical temperature T_c of its superconducting electrodes. Above T_c, the ion is experiencing an electric field noise which originates from the bulk properties of two meander-shaped resistors. In such a way, we demonstrate that our setup can be used to measure non-invasively the resistivity of the superconductor. Furthermore, it allows to observe the superconducting transition without direct electrical probing. Below T_c, the resistance of the meanders vanishes and the ion probes the noise from the surface of the trap. In this regime we measure the surface noise with a deviation from the expected power-law dependence in the frequency domain. Such a crossover regime is generally predicted [7] by the two-level fluctuator (TLF) models. However, a detailed analysis shows that TLF models cannot account for the temperature dependence of our data. Our data emphasize the need for new, refined models for the origin of electric field noise above the surface of the electrodes.

Our work is also the first attempt to use a high temperature superconductor with the transition temperature of YBCO $T_c \sim 90\,\mathrm{K}$ for microfabricated surface ion traps. Hence, in order to achieve all benefits of superconducting material only a liquid nitrogen setup is required. Trap electrodes and leads with low resistance and hence low level of Johnson noise are interesting for the fabrication of large scale ion-based quantum computers. In this work we demonstrate negligible Johnson noise from very long and thin superconducting traces placed directly on-chip. This shows that the concept of a surface ion trap based on high-temperature superconducting material can serve as a blueprint for a complicated chip designs with integrated electronics. Some parts of this chapter are extracted from the article [26].

5.1 YBCO, a high-temperature superconductor

The effect of zero electrical resistance in some materials below a characteristic critical temperature T_c is called superconductivity. It is also characterized by the complete

exclusion of magnetic fields from the volume of the superconductor, which is called Meissner effect [60]. For the first time the effect of superconductivity below 4.2 K has been observed by Kamerlingh Onnes in 1911. The resistivity of mercury dipped into liquid helium jumped to immeasurably small values (less the $10^{-5}\,\Omega$) within the small temperature range $\Delta T \sim 0.01\,\mathrm{K}$ Figure 5.1 [61].

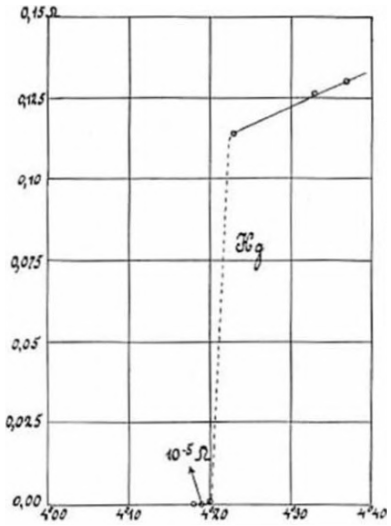


Figure 5.1: Measured resistance of mercury versus temperature. The first ever observed superconducting transition of material [61].

Superconductors are divided into superconductors of type-I and type-II, according to their behavior in magnetic fields. The first type superconductor is characterized by a critical magnetic field B_c. In magnetic fields exceeding B_c, a type-I material turns into a normal conductor. Type-II superconductors are characterized by two critical magnetic fields B_{c1} and B_{c2}. With external magnetic fields less then B_{c1}, the Meissner effect can be observed. For magnetic field values between B_{c1} and B_{c2}, a partial penetration of the magnetic field into the superconductor takes place. In type-II superconductors above B_{c2} there is a transition to a normal metal. Type-II superconductors include alloys and metals which have a high resistivity in the normal state.

Superconductivity can be explained by the Bardeen-Cooper-Schrieffer theory [62]. It is based on the concept of Cooper pairs, the bound state of two electrons interacting via a phonon. The founders of this theory received the Nobel Prize in Physics in 1972. However, the complete microscopic theory of superconductivity does not exit yet. For example, the mechanisms of high-temperature superconductivity remain unclear. Such superconducting

materials are characterized by critical temperatures T_c higher then the boiling point of nitrogen.

In 1987 a group of scientists from the University of Houston (USA) discovered that YBCO becomes superconductor at 93 K [63]. The magnetic susceptibility and resistance goes down abruptly to immeasurably small values, indicating a transition to the superconducting state. The change in the magnetic susceptibility upon cooling in a small magnetic field indicates a type-II superconductivity.

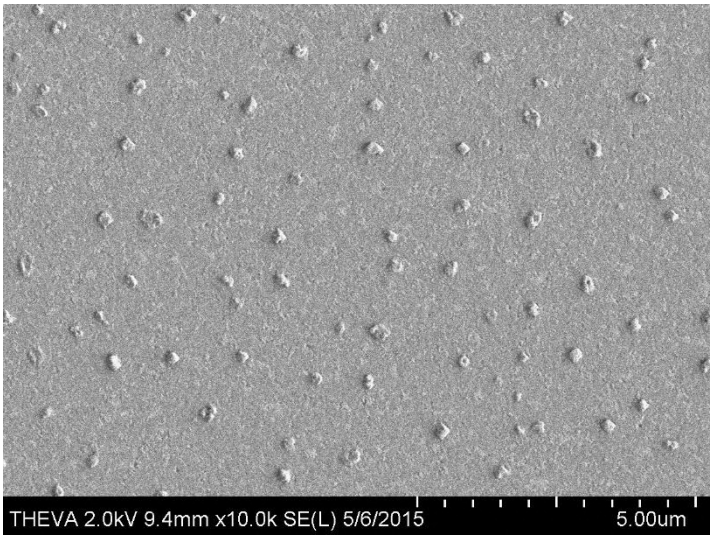


Figure 5.2: SEM picture of YBCO surface obtained after deposition. Figure courtesy of Robert Semerad.

For completeness we add additional information related to the properties of YBCO. According to the specifications given by the producer, Ceraco ceramic coating GmbH [64], the stoichiometry of the YBCO film used in the experiment is $YBa_2Cu_3O_7$ (almost complete oxygen loading). The film is S-type [a] and has a thickness of 50 nm. The film is grown on sapphire Al_2O_3 substrate with a 40 nm thick buffer layer of CeO_2. The specified critical temperature $T_c = 85.6(5)$ K, measured by Ceraco directly after fabrication, agrees with our data obtained in-situ with a 4-wire resistance measurement, $T_c = 85(1)$ K. For E-type films, the stoichiometry is very close to 1:2:3 composition. For S-type films, Ceraco

[a] S-type, M-type and E-type are standard denomination given by Ceraco specifications (http://www.ceraco.de/). The company produces three types of YBCO films: M-type, S-type and E-type. M-type is intended for **M**icrowave applications, S-type for **S**QUIDS and E-type for multilayers (**E**pitaxy) or nanowires.

increases the Copper content by 2-3% which leads to copper oxide precipitates on the surface. In case of M-type films, they increase the content of both Copper and Yttrium. Yttrium excess leads to pores visible in SEM. For M-type films Ceraco has a broad window of composition. All other parameters of fabrication (temperature, oxygen, pressure, etc) are the same, regardless of the film type. All YBCO films are single crystalline, c-axis normal to surface and in-plane oriented. The surface of S-type film has smooth matrix and small CuO_x segregations as shown on a scanning electron microscope (SEM) picture obtained directly after production; see Figure 5.2. The S-type film has been chosen because of a rather high transition temperature and because of its surface properties.

5.2 YBCO electrode trap chip

The following requirements of the chip design have to be fulfilled:

1. Below the superconducting transition the heating rate of the ion has to be limited by the noise from the surface of the trap. All other noise sources have to be negligible.

2. The superconducting transition measured with the ion should be clearly observable. The heating rate below T_c should be significantly smaller then the heating rate above T_c.

3. Above the superconducting transition, the ion should experience a measurable level of the Johnson noise. In order to correctly compare noise levels above and below T_c, we want to use the same measurement method.

The heating rate, which the ion senses above the trap surface can have different origins such as technical noise, Johnson noise from the electrodes and other parts of electrical circuit, surface properties *etc.* [6]. In the following, we want to give an assessment of the upper and lower bound for the heating rate below the superconducting transition for a particular setup. We want to make sure that the level of the Johnson noise above the transition in our trap chip is dominating all other noise sources.

Various surface ion traps with 230 µm electrode-ion separation at the temperature 10 K [9, 44] have been characterized in the same setup used for the YBCO traps, and give us a point of comparison. The surface ion traps made out of a gold-coated silicon substrate showed a record low heating rate $\Gamma_h = 0.33$ phonons/s [9]. Several other silicon-based

surface ion traps of the same size but with slightly different microfabrication processes showed on average a heating rate of ~ 1 phonons/s [44] for an axial frequency $\nu = 1$ MHz. The surface ion trap of the same geometry but made out of the gold-coated silica substrate [44] demonstrated a heating rate of $41(5)$ phonons/s at 10 K, which is the highest value observed observed in silicon traps for 230 µm electron-ion separation. We take this value as an upper bound of the heating rate at 10 K for the calculations below.

The expected temperature scaling from 10 K to 80 K was estimated from experiments [65, 54]. Both of these experiments operated with gold surface ion traps, they detected an increase of the heating by at least one order of magnitude in the temperature range from 10 K to 100 K. From this, we estimate an upper bound for the expected heating rate at the superconducting transition $T_c \approx 85$ K of $\Gamma_h \approx 400$ phonons/s. Hence according to equation (3.1), this corresponds to an electric field noise spectral density $S_{T_c} \approx 3 \times 10^{-12}\,\mathrm{V^2 m^{-2} Hz^{-1}}$.

In order to produce a sufficient amount of Johnson noise above the transition we connect a resistor R_{meander} to one of the DC electrodes, as is depicted on the Figure 5.3 (1). The expected upper bound for the required noise level above the superconducting transition is given by $S_E^{(\mathrm{JN})} = 10 \times S_{T_c} \approx 3 \times 10^{-11}\,\mathrm{V^2 m^{-2} Hz^{-1}}$. The estimated value of the resistor, generating this level of noise, can be found by using equation (3.3) with the characteristic distance δ_c calculated for the given electrode. The details of the simulations can be found in the Master's thesis of D. Schärtl [27]. In order to reach the required value of $S_E^{(\mathrm{JN})} = 3 \times 10^{-11}\,\mathrm{V^2 m^{-2} Hz^{-1}}$ a resistor of roughly $\sim 1\,\mathrm{M\Omega}$ has to be connected to the DC electrode. Such a large resistor can be included as a wire directly on the trap chip. In this case the 300 mm long wire with 50 nm thickness and 10 µm width has to be attached to the DC electrode. Large resistance of such wire creates a major obstacle for the suppression of RF pickup voltage on the DC electrode above the superconducting transition, which will be described in the next section.

RF pickup on the DC electrode

One of the important requirements for designing a surface ion trap is to ensure that DC electrodes are RF grounded. As we will see later in this section, required for this project large resistance of electrodes could cause problems for the RF grounding of the DC electrodes. In this case RF pickup occurs on the DC electrodes, which manifests itself as an additional RF voltage V_{pickup}. RF pickup can lead to excessive micromotion, reduction of the trap depth and in the worst case it can hinder trapping of an ion.

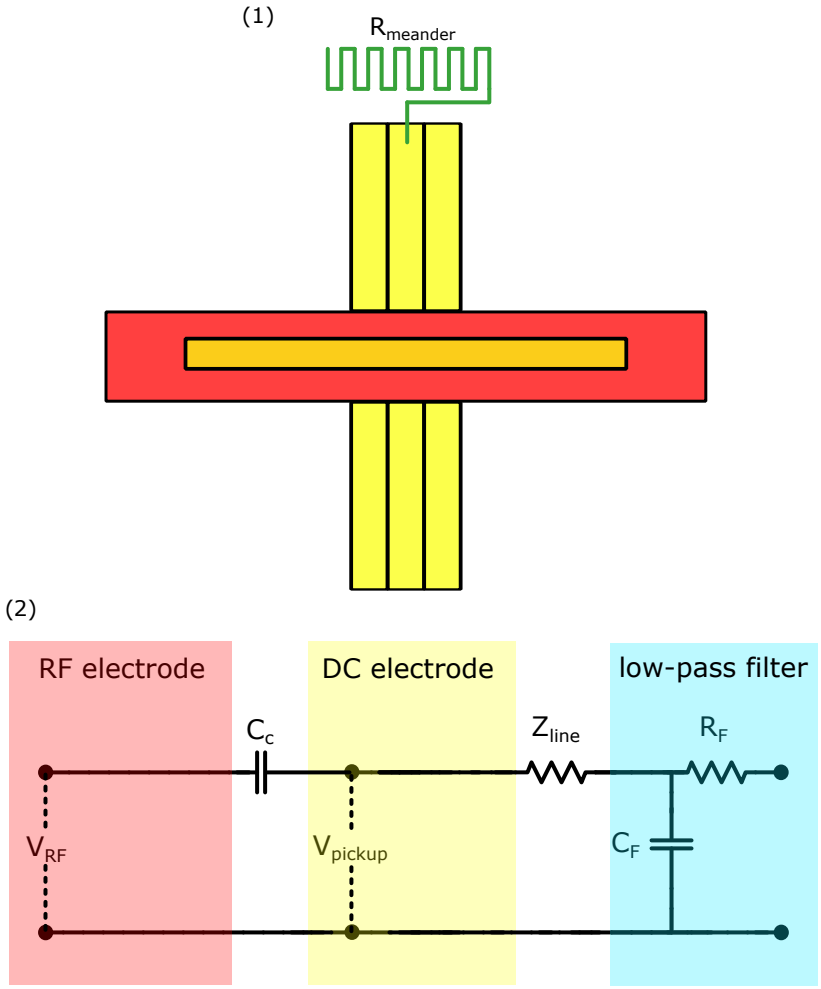


Figure 5.3: (1) The layout of the trap with the connected meander to one of the DC electrodes. Yellow color represents DC electrodes and red color represents RF electrodes. (2) The schematic electrical circuit of the RF pick up associated with one of the DC electrodes. The RF voltage (V_{RF}) is applied to the RF electrode (red box). This RF electrode is coupled to the DC electrode (yellow box) via capacitance C_{c}. On the other side of the scheme a DC voltage supply connected to the DC electrode through the low-pass filter (blue box), which consists of R_{F} and C_{F}. The DC supply is not represented on the picture because we consider only RF signals. The value of RF pick up (V_{pickup}) on the DC electrode will depend on the impedance (Z_{line}) of the connection line.

RF pickup on DC electrodes can be explained by considering the circuit shown in Figure 5.3 (2). The electrical circuit consists of an RF electrode with applied RF voltage V_{RF}, the DC electrode, RF pickup voltage V_{pickup} and low-pass filter C_{F} and R_{F}. This

RF electrode is coupled to the DC electrode via capacitance C_c. In order to estimate the influence of RF pick up we calculate the ratio between RF pickup voltage V_{pickup} and RF drive voltage V_{RF}:

$$\left|\frac{V_{\text{pickup}}}{V_{\text{RF}}}\right| = \left|\frac{(Z_{C_F} + Z_{\text{line}})}{(Z_{C_F} + Z_{\text{line}}) + Z_{C_C}}\right|, \tag{5.1}$$

where $Z_{C_F} = 1/(i\omega C_F)$ and $Z_{C_C} = 1/(i\omega C_C)$. We neglect capacitive coupling between DC electrode and the ground plane of the trap chip. Z_{line} is the total impedance of the line between C_F and C_C, that includes the resistance of the meander R_{meander} connected to the DC electrode (see Figure 5.3). One can see from equation (5.1) that if $(Z_{C_F} + Z_{\text{line}}) \ll Z_{C_C}$ the RF pickup is negligibly small.

For this project two general cases of RF pickup have to be considered:

1. $T < T_c$. The YBCO meander is in the superconducting state and $R_{\text{meander}} = 0$. The Z_{line} impedance includes residual resistance of PCB traces and bond wires and is estimated to be a few Ω. We have $|Z_{C_C}| = 1/(\omega C_C) \approx 8\,\text{k}\Omega$ for $C_C = 0.1\,\text{pF}$ [27] and RF drive frequency $\omega_{\text{RF}} = 2\pi \times 20\,\text{MHz}$. In that case RF pickup is negligible because $(Z_{C_F} + Z_{\text{line}}) \ll Z_{C_C}$.

2. $T > T_c$. For this project the resistance of R_{meander} above the superconducting transition is $\sim 1\,\text{M}\Omega$. In this case Z_{C_C} is given by R_{meander}. Therefore,

$$\left|\frac{V_{\text{pickup}}}{V_{\text{RF}}}\right| = \left|\frac{(Z_{C_F} + Z_{\text{line}})}{(Z_{C_F} + Z_{\text{line}}) + Z_{C_C}}\right| = \left|\frac{(Z_{C_F} + R_{\text{meander}})}{(Z_{C_F} + R_{\text{meander}}) + Z_{C_C}}\right|, \tag{5.2}$$

since $C_F \gg C_C$, we have $Z_{C_F} \ll Z_{C_C}$, $R_{\text{meander}} \gg Z_{C_F}$ and the ratio between V_{pickup} and V_{RF} can be rewritten as

$$\left|\frac{V_{\text{pickup}}}{V_{\text{RF}}}\right| \approx \left|\frac{R_{\text{meander}}}{R_{\text{meander}} + Z_{C_C}}\right|. \tag{5.3}$$

If we use $Z_{C_C} = 8\,\text{k}\Omega$ and $R_{\text{meander}} = 1\,\text{M}\Omega$ the ratio $\left|\frac{V_{\text{pickup}}}{V_{\text{RF}}}\right| \approx 1$. The RF pickup voltage above the superconducting transition has the same order of magnitude as the RF drive voltage. In other words, RF pick up on one of the DC electrodes would alter dramatically the trap potential, and would likely hinder a proper operation of the trap.

Two-meander design

As suggested in [27] the trap design as shown in Figure 5.4 was used to overcome the issue with enhanced RF pick up; see section 5.2. A pair of electrodes C1 and C2 are placed symmetrically with respect to the position of the ion, and connected to two identical meander-shaped structures. These meanders are made of YBCO only, without gold coating. Below T_c the resistance R_m of each meander is negligible. Above T_c the meanders' resistance R_m gives rise to Johnson noise, which translates to electric field noise at the trap center which can be sensed with an ion. This noise source can be switched on and off by adjusting the trap chip temperature. The geometry of electrodes C1 and C2 (see Figure 5.4) is designed in a such way that electric fields from correlated voltages cancel out at the center of the trap, $\boldsymbol{E}^{(C1)}(\boldsymbol{r}=0) = -\boldsymbol{E}^{(C2)}(\boldsymbol{r}=0)$, which minimizes the influence of pickup from the RF electrode by C1 and C2.

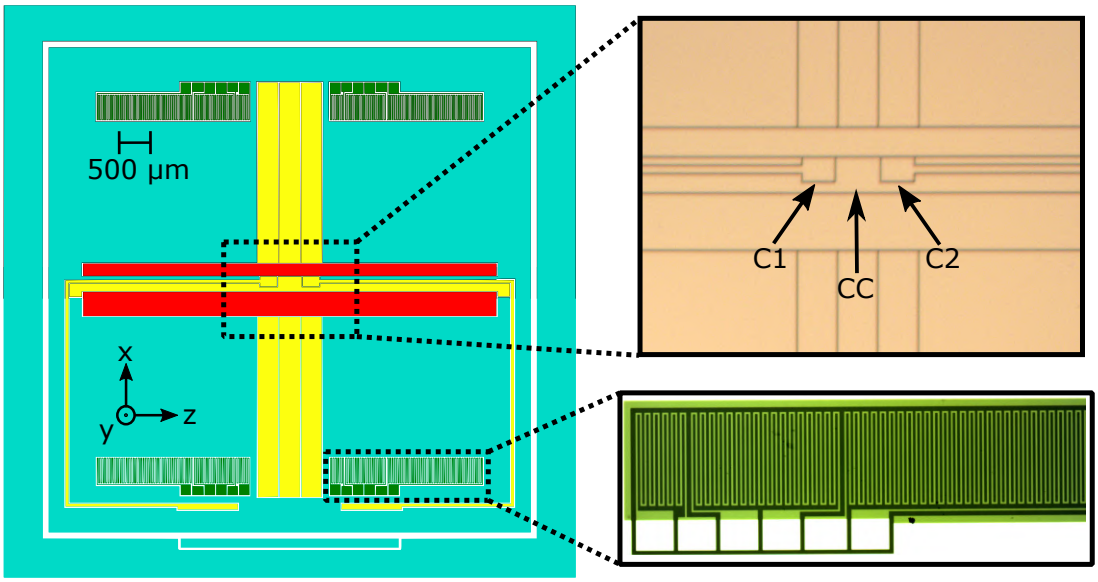


Figure 5.4: The design of the two-meander trap chip. The yellow colored polygons are DC electrodes. The red colored polygons are RF electrodes. The green colored are YBCO meanders and the remaining light blue parts are electrically grounded. The upper layer of the trap chip is covered with gold except YBCO meanders. The bottom right insert is a microscope picture of the three YBCO meanders with different length. The upper right insert is a microscope picture of the trapping region of the chip.

This design has another important property, the uncorrelated Johnson noise in the meanders adds up at the position of the ion. Hence the total electric field noise experienced

by the ion is a sum of two electric field noises from two separate meanders $S_E = S_E^{(C1)} + S_E^{(C2)}$. In order to estimate the length of the meanders we use the following equation:

$$R = \frac{\rho l}{w d}. \tag{5.4}$$

At 100 K resistivity for YBCO is $\rho_{\mathrm{YBCO}} = 131(2)\,\mu\Omega\,\mathrm{m}$ [27]. We used $w = 10\,\mu\mathrm{m}$ which is standard trace width for all our surface ion traps of that size. The thickness of the YBCO film was chosen to be $d = 50\,\mathrm{nm}$ in order to fit the criteria of meander resistance above the superconducting transition. The results of the calculation of resistance R, electric field noise S_E and heating rate Γ_{h} for the given YBCO meander length l at the temperature 100 K are listed in the Table 5.1. The levels of Johnson noise at 100 K for different meander lengths are $S_{JN}^{1,2,3} = 1.9 \times S_{T_{\mathrm{c}}}, 5.6 \times S_{T_{\mathrm{c}}}, 13 \times S_{T_{\mathrm{c}}}$ where $S_{T_{\mathrm{c}}} \approx 3 \times 10^{-12}\,\mathrm{V^2 m^{-2} Hz^{-1}}$ is the expected noise level at the superconducting transition. Such values ensure a clearly measurable transition between the normal and superconducting regimes. For all our experiments we used the smallest meander with resistance $R = 5190\,\Omega$ (at 100 K) because it gives values of the heating rate, which are measurable with the same method as below T_{c}, for the temperatures higher than 150 K.

Table 5.1: Calculated values of resistance R, electric field noise S_E and heating rate Γ_{h} for several YBCO meander lengths l with trace width $w = 10\,\mu\mathrm{m}$ and resistivity $\rho^{YBCO} = 131(2)\,\mu\Omega\,\mathrm{m}$ at temperature 100 K.

l(μm)	R(kΩ)	S_E ($\mathrm{V^2 m^{-2} Hz^{-1}}$)	Γ_h(phonons/s)
35840	94	3.99×10^{-11}	5.84×10^3
14960	39.2	1.67×10^{-11}	2.43×10^3
5190	13.6	5.78×10^{-12}	8.4×10^2

Trap fabrication

For this project we outsourced all microfabrication steps, except final chip cleaning and wire bonding. We chose Al_2O_3 (sapphire) as a substrate for several reasons. First, the thermal conductivity of sapphire at low temperatures is high and comparable with copper [27], which is crucial for proper heat transfer in our setup. Second, RF loss and dielectric constant allow us to reduce RF dissipation and reduce the coupling between RF- and DC-electrodes [27].

The thin film deposition of 50 nm of YBCO and 200 nm of gold on top of a 3-inch wafer made of 500 µm sapphire was done by Ceraco ceramic coating GmbH [64]. Specification of the YBCO film coating is presented in section 5.1.

STAR cryoelectonics [66] patterned and diced the coated wafer. Here are the different steps for patterning the wafer:

(i) Gold patterning:

  (a) Spin coating the photoresist on top of the wafer.

  (b) Photolithography.

  (c) Dry etch patterning of Au and YBCO.

  (d) Wet etching of the gold in certain areas.

  (e) Removing remaining photoresist.

(ii) YBCO patterning:

  (a) Spin coating the photoresist on top of the wafer.

  (b) Photolithography.

  (c) Argon ion milling of exposed YBCO.

  (d) Removing remaining photoresist.

(iii) Spin coating the photoresist on top of the patterned wafer to protect the surface of the chip;

(iv) Dicing of the wafer into $1 \times 1\,\mathrm{cm}^2$ individual chips.

Trap mount

The goals of this project demand several important criteria for the experimental setup. In order to measure the superconducting transition we need to heat up the trap chip as well as to measure the resistance and temperature of the YBCO meanders. To fulfill these criteria a new trap chip mount was designed and built, shown in Figure 5.5. The new design is based on the trap mount and electric PCBs, which are used for the silicon traps project; see section 4.3 and 4.3. It consists of filter boards with 16 RC low-pass filters (see section 4.3)

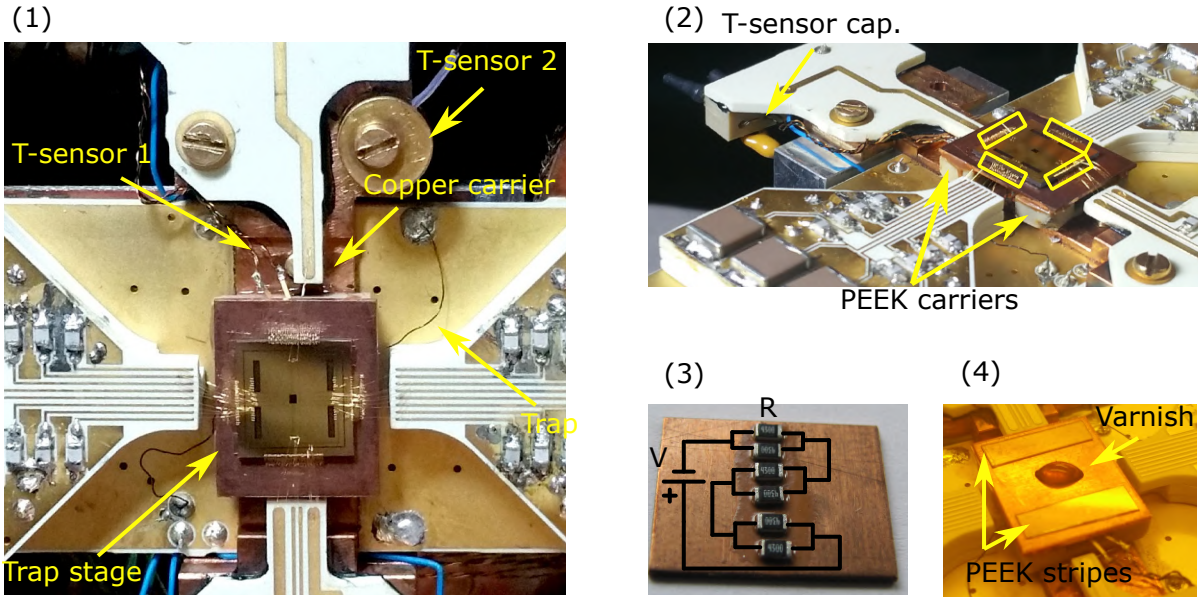


Figure 5.5: (1) Printed circuit board (PCB) with glued trap chip mounted inside of the cryostat. Temperature sensors 1 and 2 (T-sensor 1 and 2) measure the temperature of the copper carrier and of the trap stage. (2) Side view of the setup. Two polyether ether ketone (PEEK) carriers are placed in between trap stage and copper carrier. To improve thermal conductivity between the trap chip and the trap stage additional gold bonding wires have been attached, indicated in four yellow boxes. In order to minimize RF-pickup from the resonator on the temperature sensor 1.5 µF capacitor (T-sensor cap.) has been soldered. (3) The backside of the copper carrier. The local heater consists of six resistors soldered together $R_{total} = 705\,\Omega$ attached on the backside of the trap stage. (4) Two PEEK stripes on the trap stage are used to create a homogeneous layer of varnish

and a 20 MHz RF resonator (see section 4.3) and a new copper carrier [27] as shown in Figure 5.5 (1),(2).

One of the challenges of this project is to exclude the influence of technical noise on the heating rate. Large temperature gradients of the electric PCBs can modify properties of the low-pass filters and alter the resonance frequency of the RF resonator because of the temperature variation of individual components. In order to avoid such temperature gradients, the trap has to be thermally decoupled from the electric PCB. In other words, thermal conductivity between copper carrier and trap stage has to be reduced.

We use two thin stripes of PEEK [b] to support the trap chip and create a uniform

[b] polyether ether ketone (PEEK)

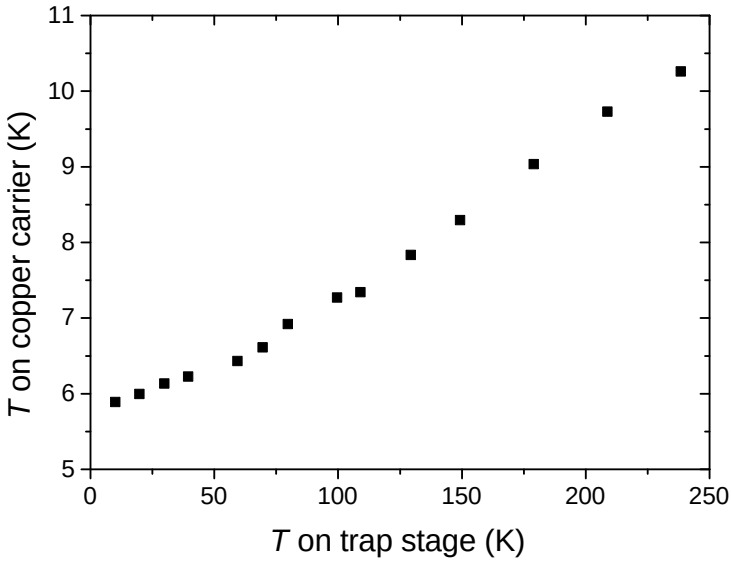


Figure 5.6: Temperature decoupling between copper carrier and trap stage. The trap stage is heated up with local heater from 10 K to 238 K. The corresponding change in the temperature of copper carrier is only 4.4 K, demonstrating good temperature decoupling. Measured data obtained without trap operation. Figure courtesy of D. Schärtl [27].

separation between copper trap stage and trap chip. The stripes have 0.125 mm thickness and 1.5 mm width and 1 cm length. The trap stage is a 20×16 mm copper plate with 0.6 mm thickness. We used a blob of the varnish [c] between the stripes and pressed the trap down Figure 5.5 (4). Such gluing procedure increases the thickness of the glue, hence reduce the mechanical stress at low temperature.

The two 3 mm thick PEEK carriers (Figure 5.5 (2)) were glued in between the copper carrier and the trap stage (Figure 5.5 (1)) with thermally conductive epoxy (EPO-TEK H74). Epoxy was cured at 150 °C to achieve nominal specifications. To increase the thermal conductivity, we thermally anchor Figure 5.5 (2) the chip and the trap stage with roughly 100 bonding wires on four different trap sides. Each anchoring bonding wire is 25 µm in diameter and $\sim$ 1 mm long. These precautions are done to avoid any temperature gradients on the chip because we want YBCO meanders (which a placed on opposite sides of the chip) switch between superconducting and normal states at the same time.

[c] Cryo-compatible varnish IMI 7031 (http://www.cmr-direct.com/)

The local heater was made out of SMD components and placed on the backside of the copper carrier (Figure 5.5 (3)). Namely, three pairs of resistors $R = 470\,\Omega$ (Yageo Europe RC1206) were glued with H74 epoxy on the bottom side of the trap stage (Figure 5.5 (3)). Each pair is soldered in parallel and connected in series in one electric circuit. The resulting resistance is $R_{\text{total}} = 705\,\Omega$. The local heater is connected to the PCB with 1 cm long wires [d]. We used the local heater to warm up the trap stage from 10 K to 238 K. As we can see in the Figure 5.6 the temperature on the copper carrier is increased by only 4.4 K. This demonstrates thermal insulation between the heated trap chip and PCB filter board.

4-wire measurement of YBCO meander resistance

In order to estimate the noise level above the superconducting transition, a 4-wire measurement method was considered and implemented into the experimental setup. The 4-wire measurement method is a standard technique for precise resistance measurement of the sample that exploits four different lines for obtaining voltage and sending current. Detailed information about the theoretical background of this method and first realization in our the experimental setup can be found in the Master's thesis of D. Schärtl [27]. For that, we directly connected YBCO meander to the Keithley 2010 multimeter for 4-wire resistance measurement. Over the course of few weeks the meander structures several times experienced a breakdown. The 10 µm wide meander line most likely was damaged with too high voltage or current applied to it. We included a 100 kΩ resistor in the current supply line of the 4-wire measurement to limit possible current overshoots but this did not solve the issue with meander breakdowns. After all, we assumed that accumulated static charges and ground loops of the 4-wire measuring circuit can damage such a delicate structure. Therefore we modified the initial 4-wire resistance measurement setup in order to fix this issue.

Modified measuring electric circuit is presented on the Figure 5.7. We used two multimeters Keysight U1251B and Agilent U1253A. These multimeters are connected to PC via IR-USB interface. Such an optical link decouples electrically the multimeter from any ground or electric circuit. These multimeters have the highest precision when used as a voltmeter. The 9 V krona battery creates voltage drop V_{battery} on the meander resistor R_{meander}. The current flowing through the meander is measured as a voltage drop on the resistor $R_{\text{current}} = 0.9152\,\text{k}\Omega$; see Figure 5.7. The RC filters are implemented to

[d] AWG phosphor Lakeshore bronze wires

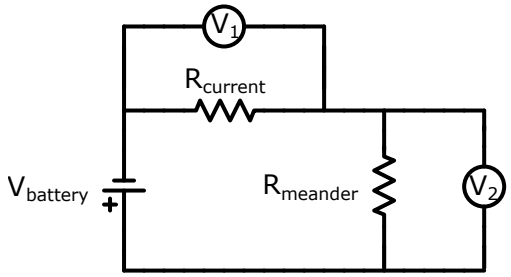


Figure 5.7: Scheme of the 4-wire resistance measurement. A 9 V krona battery is used as a voltage source. We used Keysight U1251B multimeter to measure voltage across the $R_{\text{current}} = 0.9152\,\text{k}\Omega$ and Agilent U1253A multimeter to measure voltage of the meander structure.

the circuit to decrease the meander resistance measurement error. Each individual filter consist of $0.1\,\mu\text{F}$ capacitor and $1\,\text{k}\Omega$ resistor. The cutoff frequency of the low pass filter is $f_{\text{cutoff}} = 1.6\,\text{kHz}$. In order to avoid ground loops, the measuring circuit and the RC filters were placed into the isolated aluminum box.

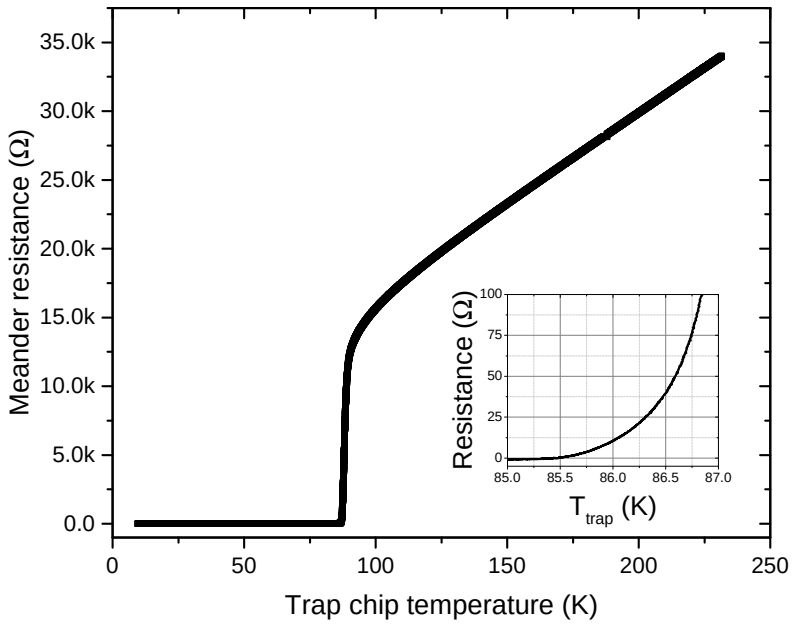


Figure 5.8: Resistance versus temperature dependence measured with 4-wire method . The superconducting transition is measured to be at $T_{\text{c}} = 86.5(2)\,\text{K}$.

5.3 First performance tests of YBCO traps

This section briefly describes the first attempt of using the YBCO trap chip and its performance characterization. We present also a short report about a failed attempt at using bypass capacitor to reduce the RF pickup.

YBCO trap without meander

For our first ion trapping experiments with a YBCO traps we used the chip design shown in Figure 5.9. It consists of seven segmented DC electrodes on each side of the RF rail which is separated by the central DC electrode. This design has the same trap electrode geometry and the same electrode-ion separation of 230 µm as the Yedikule traps [9] which allows a comparison of its heating rate with previously characterized silicon traps in the same setup [44]. The trap chip is based on the 1×1cm sapphire substrate. Electrodes are made from a 50 nm YBCO layer covered by 200 nm of gold. The chip is clamped with titanium forks to the copper stage; see section 4.3.

The heating rate of the ion is measured using the sideband ratio technique; see section 3. At the trap temperature $T = 10(2)$ K and an axial frequency $\omega_z = 1.056$ MHz the heating rate of the ion was $\Gamma_{\mathrm{h}}^{\mathrm{YBCO}} = 0.29(4)$ phonons/s. This result is consistent within the errors bars with the smallest heating rate measured on silicon-based ion trap $\Gamma_{\mathrm{h}}^{\mathrm{Si}} = 0.33(4)$ phonons/s [44]. In addition, we measured axial and radial frequency and compared it with the simulations. More detailed analysis of this trap performance is given in the Master's thesis of D. Schärtl [27].

In summary, we verified that YBCO-based surface ion traps work, meaning that the microfabrication process is reliable. We found good agreement (within 0.6 %) between measured and calculated axial frequencies [27]. The heating rate of the trap with 230 µm electrode-ion separation was as small as measured for the silicon trap [44]. Also, we conclude that the additional YBCO layer below the gold electrode does not change the heating rate of the ion.

Two-meander YBCO trap with bypass capacitor

As a next step, we glued the two-meander design trap chip (see Figure 5.4) to the trap stage of the new mount as described in the section 5.2. The two central electrodes C1 and C2 (see Figure 5.4) were connected to meanders with the expected resistance $R_{\mathrm{meander}} = 39.2\,\mathrm{k}\Omega$

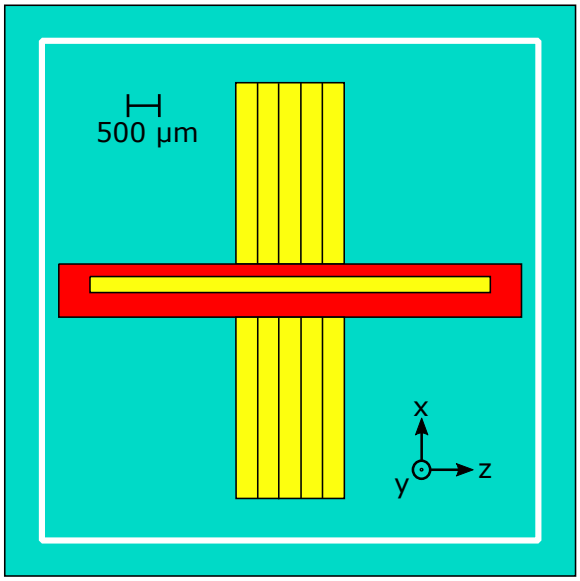


Figure 5.9: The design of the test trap chip. The yellow colored rectangles are DC electrodes. The red colored rectangular is the RF electrode.

at $T = 100\,\mathrm{K}$ (Table 5.1). Below the superconducting transition, several measurements of the heating rate have been done. For a trap temperature $T = 12(3)\,\mathrm{K}$ and axial frequency $\omega_z = 0.94\,\mathrm{MHz}$ the heating rate was $\Gamma_\mathrm{h} = 1.8(1)\,\mathrm{phonons/s}$. The next day the value of the heating rate was measured one more time for the same temperature and appeared to be $\Gamma_\mathrm{h} = 3.1(3)\,\mathrm{phonons/s}$ for the axial frequency $\omega_z = 0.87\,\mathrm{MHz}$. Also the heating rate $\Gamma_\mathrm{h} = 7.2(6)\,\mathrm{phonons/s}$ for the axial frequency $\omega_z = 0.92\,\mathrm{MHz}$ at the temperature $T = 75(10)\,\mathrm{K}$ was measured. First, these values are one order of magnitude higher than the value for the meanderless trap chip presented before. Second, the day-to-day fluctuations of the heating rate seem to indicate the presence of technical noise. Later we found that this assumption occurred to be correct; see section 5.7.

Above the superconducting transition at the temperature $T \approx 100\,\mathrm{K}$ it was possible to trap an ion. However, we observed excessive micromotion, which was not possible to compensate to a desirable level (section 2.1). This leads to the degradation of the Doppler cooling, and therefore it was not possible to cool down the ion down to the ground state with the sideband cooling. Also it was not possible to measure the heating rate with our standard technique (section 3.3). This can be caused by too high level of Johnson noise originating from the meanders' resistance $R_\mathrm{meander} = 39.2\,\mathrm{k\Omega}$. The expected level of noise at $T = 100\,\mathrm{K}$ is $\Gamma_\mathrm{h} = 2430\,\mathrm{phonons/s}$. The reason for inability to compensate

the micromotion and the inability to measure the heating rate remains unclear so far. The two-meander trap was removed from the cryostat and several modifications were implemented.

First, we decided to reduce the level of Johnson noise above the transition. The meander with the resistance $R_{\text{meander}} = 39.2\,\text{k}\Omega$ was replaced by the meander with the resistance $R_{\text{meander}} = 13.6\,\text{k}\Omega$ and expected heating rate $\Gamma_{\text{h}} = 840\,\text{phonons/s}$; see 5.4. Second, in order to minimize micromotion we integrated a bypass capacitor $C_{\text{B}} = 10\,\text{pF}$ between each meander electrode (C1, C2 on the Figure 5.4) and the ground in order to reduce RF pickup on the C1 and C2 electrodes. In the following the basic concept of optimizing RF grounding of the DC electrode is presented. The basics of RF pickup on the DC electrodes has been described in section 5.2. For temperatures $T > T_{\text{c}}$, the impedance Z_{line} (on the Figure 5.3) is given by resistance of the meander R_{meander}. The modified electric scheme with integrated C_{B} is presented in Figure 5.10 (1).

With the bypass capacitor, the ratio between RF pickup and RF drive voltage is given by the equation:

$$\left|\frac{V_{\text{pickup}}}{V_{\text{RF}}}\right| \approx \left|\frac{R_{\text{meander}}}{R_{\text{meander}}(1+\frac{C_{\text{B}}}{C_{\text{C}}})+Z_{C_C}}\right|, \tag{5.5}$$

where C_{C} is the capacitive coupling between RF and DC electrodes. So if C_{B} is high enough the RF pickup voltage V_{pickup} on the DC electrode will be suppressed. On the other hand, the bypass capacitor reduces the Johnson noise experienced by the ion because $S_E^{(\text{JN})} \propto R_{\text{eff}}$. R_{eff} is the effective real resistance which is connected to the C1 and C2 electrodes. The bypass capacitor C_{B} reduces R_{eff}:

$$R_{\text{eff}} = \frac{R_{\text{meander}}}{1+(\omega_z R_{\text{meander}} C_{\text{B}})^2}, \tag{5.6}$$

where ω_z is an axial frequency of the ion at which Johnson noise is probed. We calculate RF pickup and effective resistance R_{eff} for different bypass capacitor C_{B} values and for the following setup parameters: capacitive coupling $C_{\text{C}} = 0.1\,\text{pF}$, axial frequency $\omega_z = 2\pi \times 1\,\text{MHz}$, RF drive frequency $\omega_{RF} = 2\pi \times 19\,\text{MHz}$.

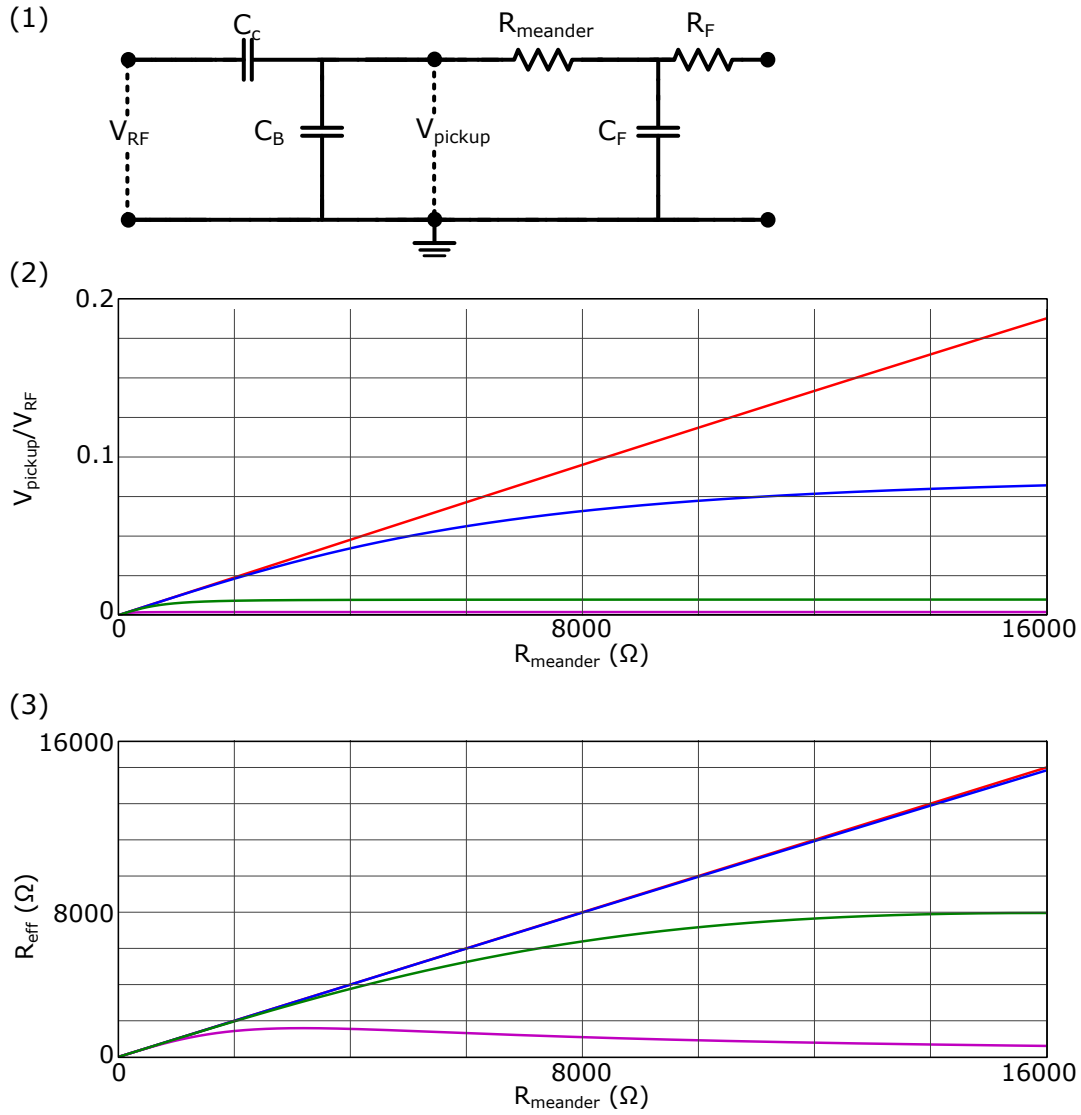


Figure 5.10: (1) Electric scheme of the improved RF grounding of the DC electrodes C1 and C2 using additional bypass capacitor C_{B}. C_F and R_F are electronic components of the low-pass DC filter. R_{meander} is the resistance of the meander structures connected to the central electrodes. C_{C} is the capacitive coupling between DC and RF electrodes. V_{RF} is a voltage of the RF drive. (2), (3) Simulations of the influence of the bypass capacitor on the RF pickup ($\frac{V_{\mathrm{pickup}}}{V_{\mathrm{RF}}}$) and on the effective real resistance (R_{eff}) of the meander [27]. The red curve represents the situation where the bypass capacitor is absent. Blue, green and purple curves correspond to the electric scheme with attached bypass capacitors $C_{\mathrm{B}} = 1\,\mathrm{pF}$, $C_{\mathrm{B}} = 10\,\mathrm{pF}$ and $C_{\mathrm{B}} = 50\,\mathrm{pF}$, respectively.

The result is shown on the Figure 5.10 (2) and (3). The optimal values for R_{eff} and $\frac{V_{\text{pickup}}}{V_{\text{RF}}}$ can be achieved with $C_{\text{B}} = 10\,\text{pF}$; see green curves on the Figure 5.10 (2), (3).

The modified YBCO chip configuration was glued to the trap mount shown in Figure 5.5 (1). Two spare low-pass filters for DC electrodes were removed from the PCB and replaced with two capacitors $C_{\text{B}} = 10\,\text{pF}$. The C1 and C2 meander electrodes were bonded with $\approx 1\,\text{cm}$ gold wires to the corresponding PCB traces with bypass capacitors. The trap was cooled to $T = 12\,\text{K}$. However, it was not possible to trap an ion. The frequencies of 397 nm and 866 nm lasers were verified with another calcium ion trapping setup. Also the fluorescence of the neutral calcium flux, $^1\text{S}_0 \longrightarrow ^1\text{P}_1$ transition, was observed on the CCD camera. In conclusion, we found no obstacles related to the electrical or optical setups, which can prevent us from trapping an ion.

Afterward, we swapped trap chip to the identical one. We did not connect the meander electrodes C1 and C2 to the bypass capacitors. Meanders with the smallest resistance $R_{\text{meander}} = 13.6\,\text{k}\Omega$ were connected to C1 and C2 electrodes. The trap chip was loaded to the vacuum chamber and cooled down to 12 K. We could load the first ion after only a few attempts. It appears that long gold wire bonds (more then 2 cm), which were connecting bypass capacitor and C1, C2 electrodes were acting as an antenna for low frequency noise, preventing ion to be trapped.

5.4 Exploiting an ion as a probe for electric field noise

By means of high-temperature superconducting meander structures it is possible to operate the trap chip, described in section 5.2, in two distinct regimes, above and below its superconducting transition T_{c}. An ion confined above such a trap chip surface can be used as probe for electric field noise. Specifically in our experiment, such a probe can detected bulk and surface properties of different materials. The bulk properties of YBCO meander structure will be covered in section 5.6 and surface properties of the gold electrode in the section 5.7.

The fact that the ion-probe can measure the resistivity of the superconductor non-invasively allows us to observe the superconducting transition without direct electrical examination. This constitutes the first observation of superconductivity using an ion as a probe. Conventional superconductors have been used in the past as ion trap material to study electric field noise above and below T_{c} [67, 68]. However, in these experiments the onset of superconductivity did not lead to a measurable modification of the electric

field noise at the ion. And, to our knowledge, it is the first time that a high-temperature superconductor is used as a material for surface ion traps.

5.5 Non-invasive measurement of the superconducting transition with an ion

The superconducting transition of the YBCO meander structure is detected and characterized with an ion non-invasively. For this, the ion's heating rate Γ_h is measured for different trap chip temperatures $T = (12 - 192.1)$K; see Figure 5.11. During the experiment the low-pass filter boards and RF resonator were kept at a nearly constant temperature $T_f \approx (10 - 14)$K; see section 5.2. All data points of the heating rate measurements for this study were done for the axial frequency $\omega_z \approx 2\pi \times 1.0$ MHz.

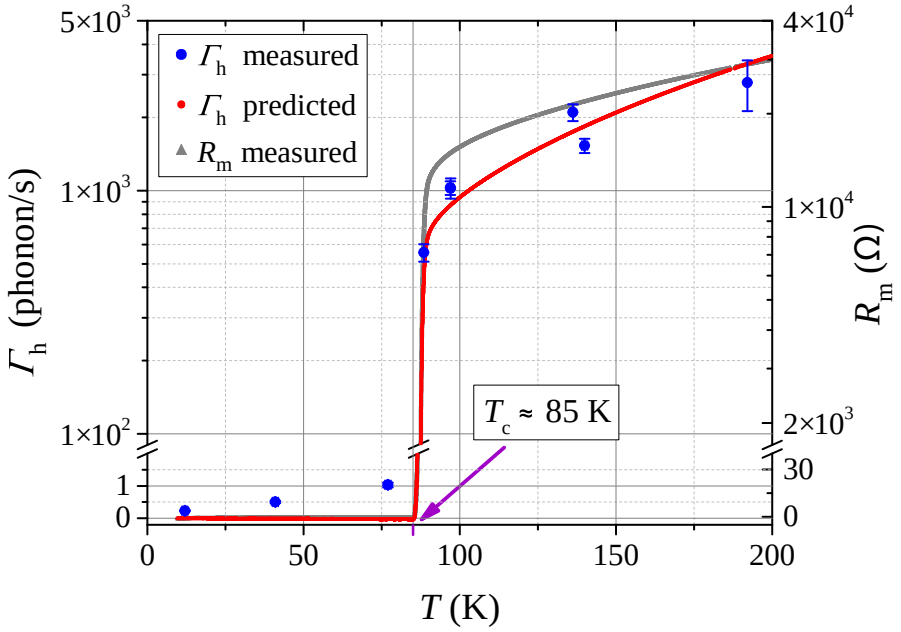


Figure 5.11: Observation of the superconducting transition of YBCO with a trapped ion. Blue dots show the measured ion motional heating rate Γ_h as a function of trap chip temperature T for a trap frequency $\omega_z \approx 2\pi \times 1.0$ MHz. The measured meander resistance R_m (gray data) is used to calculate the motional heating rate expected from Johnson noise in the meanders connected to C1 and C2 (red data). Note the break in the vertical axes.

The heating rate increases slowly below the superconducting transition from $\Gamma_h =$

$0.23(2)$ phonons/s to $\Gamma_h = 1.03(8)$ phonons/s between $T = 12\,\mathrm{K}$ and $T = 77\,\mathrm{K}$. As we will see in the following the dominant noise source in this regime originates from the gold trap surface; see sections 3.2 and 5.7. From $T = 77\,\mathrm{K}$ to $T = 89\,\mathrm{K}$ the heating rate increases sharply increases by roughly a factor 500 from $\Gamma_h = 1.03(8)$ phonons/s to $\Gamma_h = 556(46)$ phonons/s. This sudden increase corresponds to the superconducting transition at $T_c \approx 85\,\mathrm{K}$. In order to verify the transition measured with an ion we compare it with an independent 4-wire resistance measurement (Figure 5.11, gray data) identical to the one presented before in the section 5.2. Evidently, the transition on both curves occurs at the same temperature.

For $T > T_c$, we show that the ion heating rate corresponds to what is expected from Johnson noise in the YBCO meanders connected to C1 and C2. The electric field spectral density of Johnson noise is calculated using equation (3.3) where $\delta_c = 5.1\,\mathrm{mm}$ for electrodes C1 and C2 is extracted from the trap simulations [69]. Since the meanders are located directly on the trap chip, filter effects can be neglected, i.e., $R(\omega, T) = R_m(T)$. Based on the resistance and temperature measurements we calculate the expected heating rate from equations (3.1, 3.3) (Figure 5.11, red data). The measured heating rates are in good agreement with the expected values, with an average deviation $\overline{\Delta} = 1.9$. $\overline{\Delta} = \langle |\Gamma_h^{(meas)} - \Gamma_h^{(exp)}|/\sigma \rangle$, where $\Gamma_h^{(meas)}$ and $\Gamma_h^{(exp)}$ are the measured and expected heating rates, and σ is the standard deviation of an individual data point.

5.6 Measurement of the Johnson noise using an ion above the superconducting transition

When the trap chip is operated in the regime above the superconducting transition, we measured bulk properties of YBCO meander structures with an ion. Above the transition we confirmed the white-noise nature of our temperature-switchable on-chip noise source. The magnitude of the Johnson noise, which depends on the resistance of YBCO meander structures at the given temperature, verified with 4-wire resistance measurement (see section 5.2) of the reference meander structure on the chip (see section 5.2); see blue and purple solid lines on the Figure 5.12.

We measured the heating rate as a function of the axial trapping frequency ω_z for two different temperatures $T = 97\,\mathrm{K}$ and $T = 140\,\mathrm{K}$; see Figure 5.12. Solid lines show the calculated Johnson noise (see equations (3.3 , 3.1)) from the measured resistance R_m

of the reference meander structures on the chip. Dashed blue and purple lines on the Figure 5.12 account for the 1 K uncertainty in the temperature measurement. The measured data show good agreement with the calculated curves with an average deviation $\overline{\Delta} = 2.06$ for $T = 97\,\mathrm{K}$ and $\overline{\Delta} = 2.12$ for $T = 140\,\mathrm{K}$. We note that there exists another way to certify the sensitivity which uses noise injection to one of the trap electrodes [70], [71], [72] and [73]. The method presented here has the advantage that the white noise source is placed directly on chip and is therefore unfiltered.

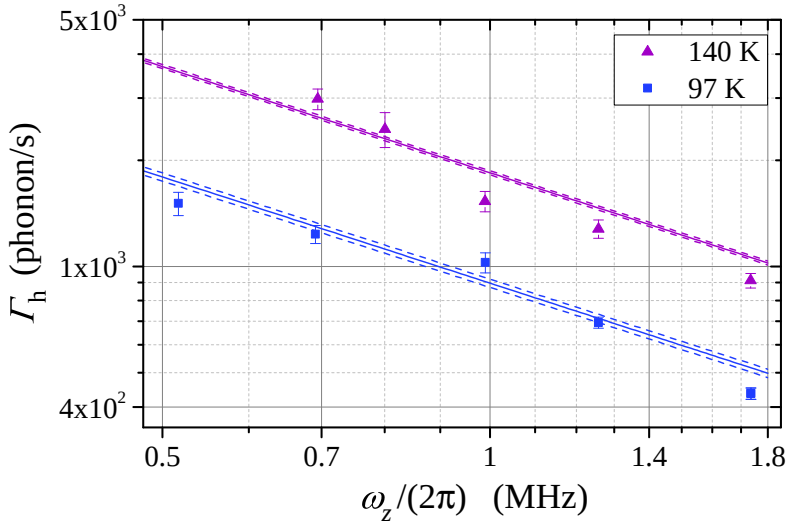


Figure 5.12: Characterization of the on-chip white-noise source above T_c using a trapped ion. Blue and purple dots show measured heating rate Γ_h as function of trap frequency for temperatures $T = (97, 140)\,\mathrm{K}$. Solid blue and purple lines are predictions for Johnson noise from the measured resistance R_m of the reference meander structures on the chip. Dashed lines reflect the 1 K uncertainty in the temperature measurement.

5.7 Observation of surface noise using an ion below the superconducting transition

In sections 5.7, 5.8 and 5.9, we demonstrate that the heating rate below the superconducting transition is dominated by surface noise. In order to support our claim, in the section 5.7 we perform a detailed statistical analysis of the obtained data. Subsequently, we exclude the most relevant technical noise sources as described in the section 5.8. We also prove

that the YBCO meander resistors do not contribute to the noise observed below T_c (within measurement uncertainties) by comparing noise levels with and without these structures, see section 5.9.

Below the superconducting transition, the heating rate spectrum is measured at three different temperatures $T = (12, 41, 77)\,\mathrm{K}$; see Figure 5.13. For temperatures $T = (12, 41)\,\mathrm{K}$ each dataset was taken over the course of one day and for temperature $T = 77\,\mathrm{K}$ the data were taken over the course of 3 days. At $T = 12\,\mathrm{K}$ and axial trapping frequency $\omega_z = 2\pi \times 1.51\,\mathrm{MHz}$ we observe $\Gamma_\mathrm{h} = 0.051(10)\,\mathrm{phonons/s}$. Such heating rate corresponds to an electric field spectral density $S_E = 5.2(11) \times 10^{-16}\,\mathrm{V^2 m^{-2} Hz^{-1}}$; see equation (3.1). These are, to our knowledge, the lowest heating rate and electric field noise observed in Paul traps so far. The absolute record of the sensitivity to electric field noise has been set very recently by the BASE collaboration in a Penning trap [74].

We examine our setup for various non-surface noise sources such as external technical noise which is independent of the trap chip temperature, in contrast to the measured heating rates. As well as Johnson noise from filters, wiring and trap electrodes is calculated to be significantly smaller than the noise we measure. Details can be found in the section 5.8.

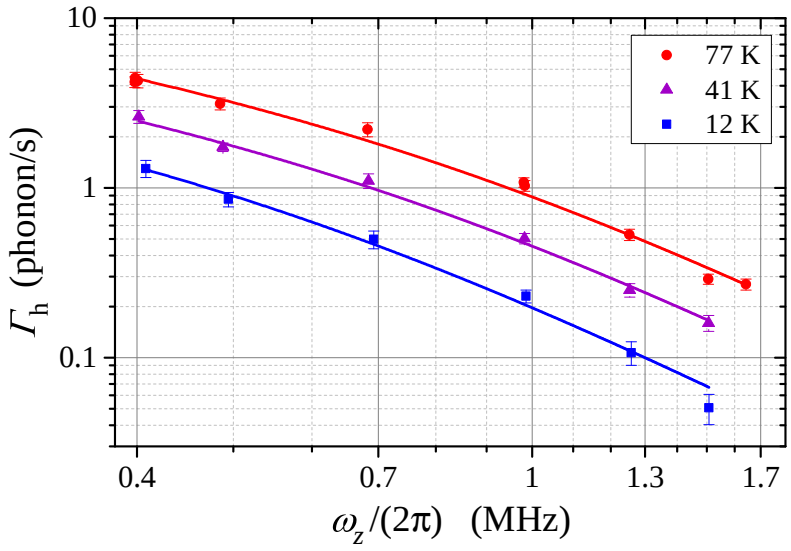


Figure 5.13: Heating rate spectra for temperatures below T_c. Blue, purple and red dots show measured heating rate as function of trap frequency for trap chip temperatures $T = (12, 41, 77)\,\mathrm{K}$. Each temperature dataset is fitted separately with the TLF model; see equation (3.4).

In this experiment, the capability of switching between two distinct regimes relies on the specific design of the trap chip. However, such unconventional trap geometry leaves an open question whether the meander structures influence the heating rate datasets below T_c. Thus we measure heating rate spectra with and without superconducting YBCO meanders on a similar trap chip; see section 5.9. The contribution of these structures below the superconducting transition was negligible within the uncertainty of our measurement.

We further analyze the spectral properties and temperature dependence of the surface noise measured below T_c. Here we show that the measured surface noise spectrum deviates from a generally expected power-law [6]. To do this we fit each temperature datasets from Figure 5.13 individually both with a power-law and with a two-level fluctuator (TLF) model; see section 3.2. The power-law is given by

$$\Gamma_h = C\,\omega_z^{-\alpha}. \tag{5.7}$$

We find an exponent $\alpha \approx 2$ for all three data sets (see table Table 5.2), corresponding to a $1/f$ frequency scaling of the electric field noise S_E; see equation (3.1). The exponent is close to the ones reported in the articles [56, 35], where a $1/d^4$ distance scaling of the heating rate was found, as is expected from the surface noise. However, a detailed analysis of the frequency dependence in the data of Figure 5.13 reveals a change in the local power-law exponent α around 0.8 MHz, which indicates a crossover between low- and high-frequency domains. This behavior is predicted by TLF models [6].

Table 5.2: Result of a power-law fit parameters C and α (equation 5.7), to the three datasets below superconducting transition; see Figure 5.13.

T(K)	α	C
12	2.3(2)	0.18(2)
41	2.0(1)	0.42(3)
77	1.9(1)	0.77(6)

In Figure 5.13 the blue, red and purple lines represent a TLF fit to the measured heating rate spectra below T_c. We use two adjustable parameters ω_0 and A in order to fit the data. Note that also for the case of a power-law fit two adjustable parameters have been used. The outcome for the TLF fit parameters is shown in the Table 5.3. The criterion that we use to determine that the TLF models fit better than the power-law is the reduced chi squared (Table 5.4), which is significantly smaller for the TLF models than for the power-law for

Table 5.3: Crossover frequency $\omega_0(T)$ and magnitude prefactor $A(T)$ resulting from the TLF models fit $S_E^{(\mathrm{TLF})}(\omega) = A\omega_0/(\omega_0^2+\omega^2)$, equation (3.4), to the spectral data in Figure 5.13.

T(K)	$\omega_0/(2\pi)$(MHz)	$A\times 10^8$(V^{2}m^{-2})
12	0.58(8)	2.0(1)
41	0.74(5)	4.1(1)
77	0.81(8)	7.8(3)

all three temperature data sets. This confirms the existence of the crossover regime in our data.

Distinguishing between different physical mechanisms may require more precise measurements than have been done until now. The fact that we can reliably distinguish between a power-law and a crossover is due to the quality and amount of our experimental data. The three data sets in Figure 5.13 necessitated a total run of more than 120,000 experimental sequences (for each frequency typically 5 delay times, each with at least 960 interleaved measurements on the blue and red sideband transitions). It is the first time that surface noise measured in ion traps shows a deviation from a power-law.

Table 5.4: Statistical evidence of the deviation from a power-law of the measured heating rate spectra below T_c, Figure 5.13. The second column shows the reduced chi squared for the power-law fit, the third column shows the reduced chi squared for the TLF models fit.

T(K)	$\chi^2_{\text{power law}}$	$\chi^2_{\text{TLF model}}$
12	2.9	1.3
41	2.4	0.8
77	6.0	2.3

The crossover frequency occurs in the range $\omega_0 = 2\pi \approx (0.6-0.8)$ MHz. The temperature dependence of the spectrum given by equation (3.4) scales as [6]

$$A(T) = A_0 \cosh^{-2}(T_0/2T)\,. \tag{5.8}$$

The temperature dependence of the TLF models does not fit the measured temperature scaling in Figure 5.13. This can be seen by applying a global TLF fit to the three measured spectra instead of fitting them individually as we do in the Figure 5.13. The global fit

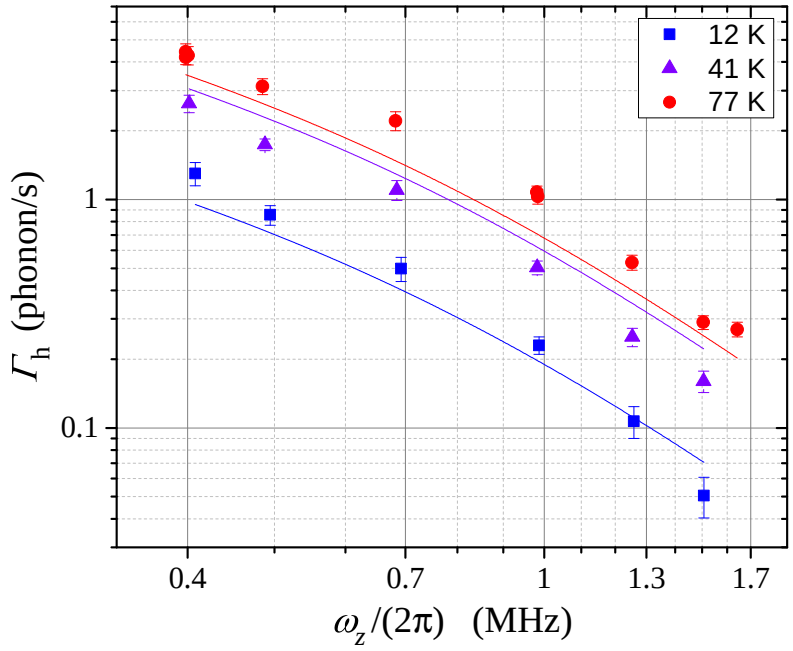


Figure 5.14: Blue, purple and red lines represent a global fit to the TLF models of the measured spectra. We use equation (5.8) with three fit parameters A_0, T_0, ω_0. We compare this with the fit from Figure 5.13 to show that we cannot explain the scaling of the magnitude of measured data.

including the $\cosh^{-2}(T_0/2T)$ scaling (Figure 5.14) significantly deviates from our data in stark contrast to the individual fits shown in Figure 5.13.

The deviation in Figure 5.14 cannot be explained by day-to-day fluctuations of the noise level because the 41 K and 77 K datasets were taken within the same cooling cycle of the cryostat within the course of 1 week. For 77 K we have repeated several frequency data points within the course of 3 days. These measurements show a heating rate variation of 5%. Also, the data for 12 K has been repeated for several frequencies within the course of a few weeks, which deviates from the value plotted in the Figure 5.13 and Figure 5.14 by roughly 10%. These measurements suggest that day-to-day variations of the measured noise were at most around (5-10)%. Therefore, such a variation is insufficient to explain the deviation between predicted and measured temperature scalings in Figure 5.14. Therefore, from the above arguments, we conclude that the measured spectra (see Figure 5.13) can be described by the spectrum of a single TLF [6] correctly. However, this approach fails to describe the temperature dependence, see Figure 5.14. A more complex model would

include averaging over a distribution of TLFs with a range of model parameters, yielding a different temperature scaling [6]. However, averaging over TLF distributions typically shows a power-law in the frequency dependence [6], which contradicts the observed crossover regime (see Figure 5.13). Nevertheless, this approach might still lead to a model that is consistent with our data. Additional heating rate measurements for different temperatures below the superconducting transition could help to obtain more knowledge about such a TLF distribution, as was shown in [75]. This might be a good topic for future generations of Ph.D. students.

5.8 Technical and Johnson noises below T_c

In this section technical and Johnson noises as dominant sources of the heating rate below superconducting transition are discussed. The following arguments prove that the noise causing the ion's motional heating below T_c originates from the surface of the trap.

External technical noise below T_c

The trap mount (see section 5.2) which is used for this project demonstrates good thermal decoupling of the heated trap chip from the filter PCB board. When the trap chip temperature is changed from 12 K to 77 K the filter PCB temperature T_f changes by roughly 1 K. This temperature change is small but might still modify the attenuation of external noise by the low-pass filter (see section 6.4). In order to exclude the influence of the temperature gradient on the filter properties we measure the transfer function of the filter for different temperatures. Note that all cryogenic DC filters in our setup are identical; see section 6.4. For all heating rate measurements we use one filter line to apply the DC voltage and a second filter line to measure it. Two filter lines are connected via gold bonds to the trap electrode. In order to measure the transfer function of the cryogenic RC filter we inject RF signal through one filter line with amplitude V_{in} and measure the attenuated signal V_{out} through an other second filter line. The resulting transfer function corresponds to that of the first order RC filter used in the experiment but with a capacitance twice as large. This additional capacitance changes the cut-off frequency of the filter $f_c \approx 4.8$ MHz by a factor of two.

On Figure 5.15 we present he measured transfer function $G = |V_{out}/V_{in}|^2$ of the low-pass filter as a function of the filter temperature $T_f \approx (10-100)$ K for three different

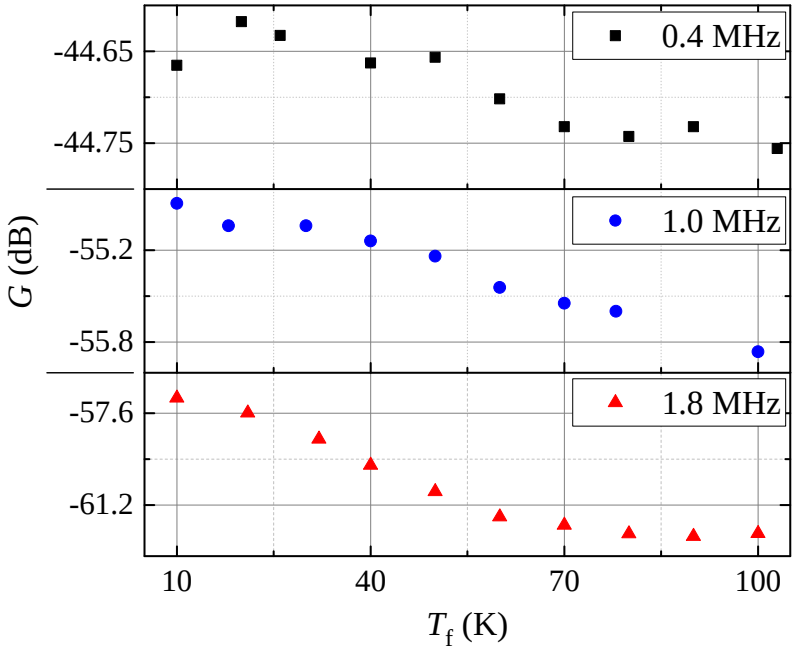


Figure 5.15: Transfer function G of the low-pass filter as a function of the filter temperature T_f for three different frequencies $\omega = 2\pi \times (0.4, 1.0, 1.8)$ MHz.

frequencies $\omega = 2\pi \times (0.4, 1.0, 1.8)$ MHz. The applied change in T_f strongly overestimates the variation in filter temperature $T_f \approx (10 - 14)$ K during the heating rate measurements. But even for stronger increase T_f, the temperature scaling of the filter attenuation does not correlate with the heating rate data shown in Figure 5.13.

Also Figure 5.13 indicates that while the temperature of the trap chip varies from 12 K to 77 K the magnitude of the measured spectra is rising from $2.0(1) \times 10^{-8}\,\mathrm{V^2 m^{-2}}$ to $7.8(3) \times 10^{-8}\,\mathrm{V^2 m^{-2}}$; see Table 5.3. But the external technical noise decreases with rising temperature, as shown in Figure 5.15. From this we conclude that the heating rate at 41 K and 77 K is not dominated by external technical noise. Furthermore, each dataset for temperatures below T_c demonstrates the same characteristic behaviour in the frequency domain. This indicates that the heating rate at 12 K has the same origin as for other temperatures below T_c.

Johnson noise below T_c

We exclude Johnson noise as dominant noise source for chip temperatures $T < T_c$. Below the superconducting transition the electric field spectral density of Johnson noise from

the trap electrodes, bonding wires, and PCB traces, which are not filtered by the low-pass filters, should have a flat frequency dependence; see equation (3.3). It contradicts with what we observe on the Figure 5.13 where we measure $1/f$ scaling of the electric field spectral density. Also, we exclude Johnson noise from the low-pass filters using a temperature scaling argument. If the trap chip is heated to $T = 77\,\mathrm{K}$, the filter temperature changes by roughly a 10% from $T = 10\,\mathrm{K}$ to $T = 11\,\mathrm{K}$, due to thermal insulation. We neglect the change in the filter resistance because of the small temperature change of the filters. From equation (3.3) Johnson noise scales linearly with temperature, hence the electric field noise produced by the filters should therefore increase by 10%. In contrast, the increase of the measured noise level in Table 5.3 from $A = 2.0(1)\,\mathrm{V^2/m^2}$ at $T = 12\,\mathrm{K}$ to $A = 7.8(3)\,\mathrm{V^2/m^2}$ at $T = 77\,\mathrm{K}$ corresponds to a change by roughly a factor 3.9, more than one order of magnitude larger than the change calculated from Johnson noise of the low-pass filters.

In addition to the arguments above, we calculate upper bounds for Johnson noise from trap electrodes, wiring, and low-pass filters for highest temperatures below T_c. The resulting Johnson noise $S^{(\mathrm{JN})}_{E,80\,\mathrm{K}}$ is an upper bound for the Johnson noise expected at the three temperature sets in Figure 5.13, since the total resistance will decrease at lower temperatures. Each electrode is connected to a resistance $R_\mathrm{tot} = R_\mathrm{elec} + R_\mathrm{wire} + R_\mathrm{filter} \approx (102 \text{ to } 164)\,\mathrm{m\Omega}$, where the individual contributions are calculated below. The electric field noise S_E produced by the resistance R_tot at the position of the ion is given by equation (3.3). From this we calculate an electric field noise level $S^{(\mathrm{JN})}_{E,80\,\mathrm{K}} \approx 6.0 \times 10^{-17}\,\mathrm{V^2 m^{-2} Hz^{-1}}$ at $T = 80\,\mathrm{K}$. $S^{(\mathrm{JN})}_{E,80\,\mathrm{K}}$ is roughly a factor 50 smaller than the noise corresponding to the smallest heating rate $\Gamma_\mathrm{h} \approx 0.3\,\mathrm{phonons/s}$ we measure at $T = 77\,\mathrm{K}$. Also, $S^{(\mathrm{JN})}_{E,80\,\mathrm{K}}$ is still about an order of magnitude smaller than the smallest noise level $S_E = 5.2(11) \times 10^{-16}\,\mathrm{V^2 m^{-2} Hz^{-1}}$ we measure at $T = 12\,\mathrm{K}$. This shows that Johnson noise from these sources is negligible compared to the measured noise. The details of the calculation of R_tot are given in the following.

All DC trap electrodes are connected individually to their first order RC filter via a gold wire bond connection and a gold-plated copper trace on the filter PCB. Electrodes C1, C2 are singly bonded, all other electrodes are doubly bonded. The wire bonds have a diameter of 25 µm and a length of roughly 2 cm. A single wire bond's resistance at $T = 80\,\mathrm{K}$ is then $R_\mathrm{wb} \approx 50\,\mathrm{m\Omega}$, using a typical resistivity $\rho_\mathrm{Au} \approx 0.48 \times 10^{-8}\,\Omega\,\mathrm{m}$ at that temperature [76]. Typical values for contact resistances from chip to wire bond and from wire bond to PCB trace produced by our wedge bonder are $R_\text{wb-chip} \approx 46.0(2)\,\mathrm{m\Omega}$, $R_\text{wb-PCB} \approx 28.5(2)\,\mathrm{m\Omega}$,

measured at room temperature in a 4-wire configuration. For the further calculation we assume that the contact resistances do not change with temperature.

The PCB traces have a width of 300 µm, a thickness of 100 µm and a maximal length of 2 cm to the first filter capacitor. The trace thickness is larger than the skin depth in copper $\zeta_{\mathrm{Cu}} \approx 26\,\mu\mathrm{m}$ at $\omega = 2\pi \times 1.8\,\mathrm{MHz}$, calculated for a typical resistivity $\rho_{\mathrm{Cu}} \approx 0.22 \times 10^{-8}\,\Omega\,\mathrm{m}$ at $T = 80\,\mathrm{K}$ [76] and $\mu = \mu_0$. Therefore we use twice the skin depth instead of the trace thickness to calculate the trace resistance $R_{\mathrm{tr}} \approx 3\,\mathrm{m}\Omega$ at $T = 80\,\mathrm{K}$. The total resistance of the wiring connected to electrode C1 (or C2) at $T = 80\,\mathrm{K}$ is then $R_{\mathrm{wire}} = R_{\mathrm{tr}} + R_{\text{wb-PCB}} + R_{\text{wb-chip}} + R_{\mathrm{wb}} \approx 126\,\mathrm{m}\Omega$. For all other electrodes the bond and contact resistances have to be replaced by half the value such that $R_{\mathrm{wire}} \approx 64\,\mathrm{m}\Omega$ because of the double bond connection.

Let us consider resistors R_{C3}, R_{C4} which are modeling the equivalent series resistance (ESR) of the capacitors C_3 and C_4 of the RC filter, see Figure 4.4 (1). The resistances R_2, R_{C3}, R_{C4} within the RC filter are another source of Johnson noise. The corresponding electric field noise is calculated by considering the effective real resistance $R_{\mathrm{filter}} = R_{\mathrm{eff}}$ of the circuit from the perspective of the trap electrode [6]. For the filter circuit shown in Fig. Figure 4.4 (1) the effective real resistance is given by

$$R_{\mathrm{eff}} = \mathrm{Re}\left\{\left(\frac{-i}{\omega C_{\mathrm{el}}}\right) \parallel \left(R_{\mathrm{C4}} - \frac{i}{\omega C_4}\right) \parallel \left(R_{\mathrm{C3}} - \frac{i}{\omega C_3}\right) \parallel R_2\right\}, \tag{5.9}$$

where $a \parallel b$ denotes the impedance of two elements a, b in parallel. The capacitance of the trap electrode to ground C_{el} is on the order of 1 pF. The ESR of the filter capacitors is frequency dependent. Within the relevant frequency range $\omega_z = 2\pi \times (0.4 - 1.8)\,\mathrm{MHz}$ the maximal ESRs are $R_{\mathrm{C3}} = 24(1)\,\mathrm{m}\Omega$ and $R_{\mathrm{C4}} = 1.3(1)\,\Omega$ according to the room temperature specification of the capacitors. This gives rise to a maximal effective real resistance $R_{\mathrm{filter}} = R_{\mathrm{eff}} = 38(1)\,\mathrm{m}\Omega$.

In order to give an upper bound for the level of Johnson noise produced the by trap electrodes we neglect the influence of the electrodes' gold top layer. This assumption is justified because the resistivity of gold is much higher than the resistivity of the YBCO film below it, which is small but finite in the RF domain, even below T_c [77]. The surface resistivity of the 50 nm thick YBCO film at $f = 10.9\,\mathrm{GHz}$ and $T = 10\,\mathrm{K}$ is $\varrho_{\mathrm{YBCO}} \approx 0.66\,\mathrm{m}\Omega$ ((value specified by Ceraco $\varrho_{\mathrm{YBCO}} \approx 0.1\,\mathrm{m}\Omega$ for 330 nm thickness and $T = 10\,\mathrm{K}$, $f = 10.9\,\mathrm{GHz}$). As a next step we calculate a surface resistivity $\varrho_{\mathrm{YBCO}} = 1.8 \times 10^{-11}\,\Omega$ at $f = 1.8\,\mathrm{MHz}$ and $T = 10\,\mathrm{K}$ [78]. We use a temperature scaling $\varrho \propto (T/T_c)^2/\sqrt{1-(T/T_c)^4}$, [79], to calculate a surface resistivity $\varrho_{\mathrm{YBCO}} = 3.4 \times 10^{-11}\,\Omega$ at $f = 1.8\,\mathrm{MHz}$ and $T = 80\,\mathrm{K}$.

At the same time, the 200 nm thick Au top layer even at $T = 10\,\mathrm{K}$ still has an estimated surface resistivity of $\varrho_{\mathrm{Au}} = 1.1\,\mathrm{m\Omega}$ [76]. From the surface resistivity of YBCO we estimate the resistance of the trap electrodes for our trap geometry. Here we present an example of the calculation for one of the meander-shaped electrodes, which have the largest resistance. These electrodes have a length $l = 5.18\,\mathrm{mm}$ and a width $w = 10\,\mu\mathrm{m}$. The total meander resistance at $f = 1.8\,\mathrm{MHz}$ and $T = 80\,\mathrm{K}$ is then $R_{\mathrm{m}} = l\varrho_{\mathrm{YBCO}}/w = 17.8\,\mathrm{n\Omega}$. This is 7 orders of magnitude smaller than the resistance R_{wire} of the wiring. Since the resistances of the other trap electrodes R_{elec} are much smaller, their contribution to the Johnson noise is, like that of the meanders, negligible.

5.9 Meander-less measurement

We rule out any kind of potential effects of the YBCO meander structures connected to DC electrodes C1 and C2 on the ion heating rate below T_{c}. For example, such effects as electromagnetic pickup noise in the meander structure. We exclude any other potential effects of the superconducting YBCO meanders connected to C1 and C2 on the ion heating rate below T_{c}, like for instance electromagnetic pickup noise in the meander structure. For this we use a second, similar trap chip on which the central trap region does not have gold coating so an ion can be directly exposed to the YBCO surface. Other than that, the trap topology is identical to the trap which is used in the experiments above. For more details see the Ph.D. thesis of P. Holz [80].

In Figure 5.16 (blue triangles) we present a heating rate spectra with connected meander structures for three different temperatures $12\,\mathrm{K}, 37\,\mathrm{K}, 83\,\mathrm{K}$ (same configuration as for the experiment in the sections 5.7, 5.6, 5.5). We found that all spectra show a clear power-law dependence in the frequency domain. Afterward, we opened the cryostat in order to change trap chip wiring. Wire bonds connecting meanders and C1, C2 electrodes were removed. Then we directly connected C1, C2 with filter PCB. Spectra for temperatures $12\,\mathrm{K}, 40\,\mathrm{K}, 83\,\mathrm{K}$ show the same spectral behavior as for connected meanders; see blue and green data in Figure 5.16. We conclude that no difference between these two configurations (with and without meanders) is observed. We found in both cases a heating rate $\Gamma_{\mathrm{h}} = 0.7(1)\,\mathrm{phonons/s}$ at $\omega_z = 2\pi \times 1.0\,\mathrm{MHz}$ and $T = 14\,\mathrm{K}$, comparable to the value $\Gamma_{\mathrm{h}} = 0.23(2)\,\mathrm{phonons/s}$ at $\omega_z = 2\pi \times 1.0\,\mathrm{MHz}$ and $T = 12\,\mathrm{K}$ in Figure 5.13.

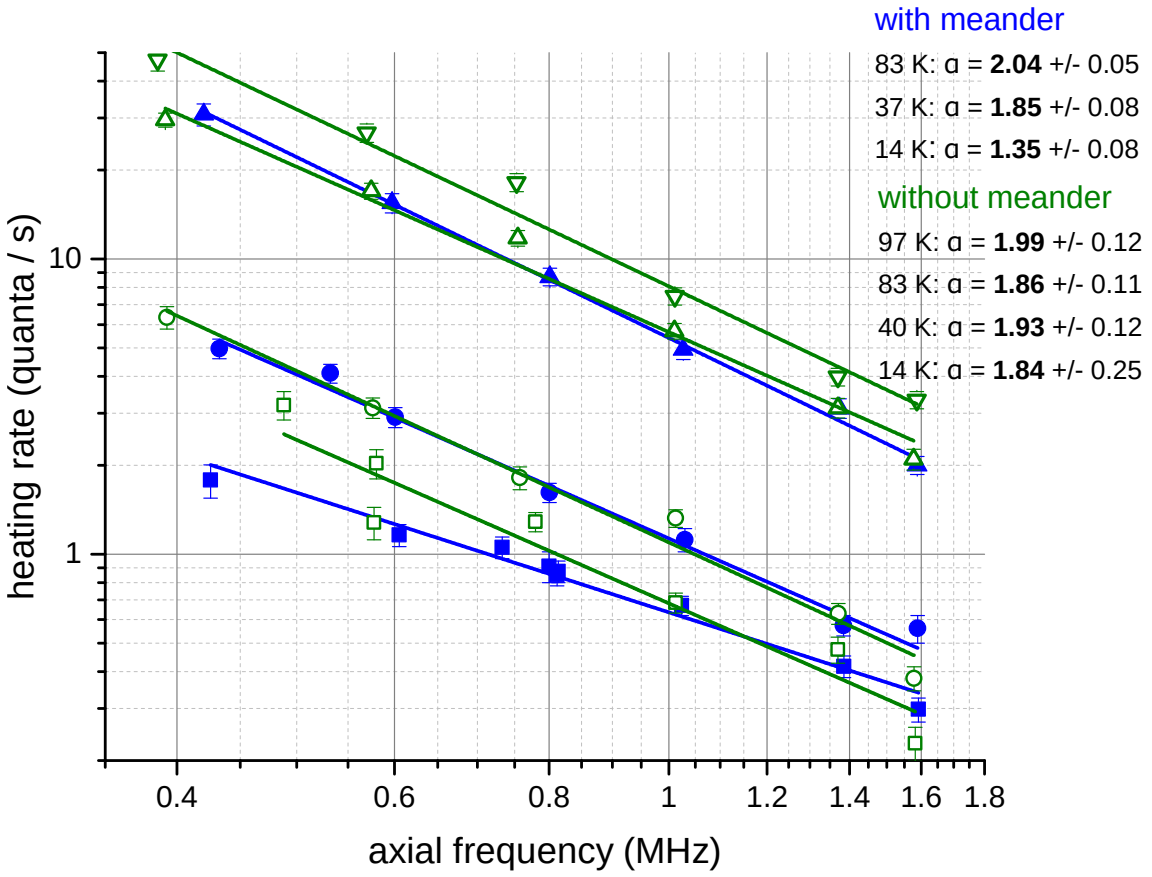


Figure 5.16: Heating rate spectra for temperatures below T_c and for one above. Green and blue triangles show measured data without and with meander respectively. Green and Blue lines represent a linear fit of each temperature data set with and without meanders. For this experiment, a specially designed trap with an exposed YBCO area below the ion is used. We don't have a good hypothesis to explain the frequency scaling exponent for $T = 14\,\mathrm{K}$ for the measurement with meander, which deviates from the one observed at the other temperatures.

CHAPTER 6

Silicon surface ion traps

In this chapter, we discuss the promising fabrication technique for surface ion traps, which is based on the usage of patterned intrinsic silicon. The method features several advantages. This method allows for producing a clean electrode surface in a very simple way, which can be an important factor for the reduction of the heating rate of the trapped ion [6]. As it was shown before, such trap chips demonstrate record low heating rates $\Gamma_h = 0.33\,\text{phonons/s}$ for electrode-ion separation of $230\,\mu\text{m}$ [9]. Another advantage of silicon-based surface ion traps is the availability of modern microfabrication technology, like micro-electro-mechanical systems (MEMS).

The chapter is arranged as follows. In section 6.1 basic operation principles of silicon-based surface ion traps will be explained. Details of chip design and the difference in fabrication processes in FH Vorarlberg (FHV) and Infineon will be covered in sections 6.2, 6.3. Results of the study of the trap chips with various electrode-ion separation are presented in section 6.6. It is followed by an explanation and detailed study of light-induced charge carrier effect; see sections 6.5, 6.7. Such an effect creates a major obstacle for silicon-based traps. Conclusion and future perspectives of silicon-based surface ion traps are summarized in section 7.

6.1 Intrinsic silicon as a substrate for ion trapping

As described in chapter 2, an RF signal has to be applied to the electrodes of the trap chip in order to confine an ion. This imposes a strict requirement on the chip substrate. Namely, it is crucial that the chip substrate has low RF losses. In the following section, we characterize RF losses in silicon substrates and we describe the methods allowing us to minimize them.

In general, RF loss in a capacitor can be characterized by the energy dissipation in one oscillation cycle, which is $1/Q$, where Q is the quality factor. The dissipation rate can also be described in terms of the loss tangent $\tan\delta = 1/Q$. In case of a semiconductor, the loss tangent $\tan\delta$ is described by

$$\tan\delta = \tan\delta_d + \frac{1}{\rho\omega\epsilon_0\epsilon_r}, \tag{6.1}$$

where $\tan\delta_d$ is the dielectric loss tangent, ρ is the resistivity of the semiconductor, ω is the angular frequency (RF frequency in our case), ϵ_0 is the permittivity of the vacuum and ϵ_r is the relative real permittivity of the semiconductor [81]. Dielectric loss tangent relates to the pure dielectric loss mechanisms such as electronic or ionic polarization. A high $\tan\delta_d$ causes heating of the trap chip and reduces the resonator quality factor, which lowers the voltage step-up factor. At RF frequencies the dielectric loss tangent in silicon is mainly given by the resistivity. Intrinsic silicon at room temperature is characterized by a large resistivity higher than $5000\,\Omega\,\mathrm{cm}$. This provides a loss tangent of 1.5 at typical trap drive frequency of 20 MHz [9]. In general, it is impossible to achieve sufficient trap operation with such RF losses.

Several methods are known to utilize fabrication capabilities of silicon and at the same time to avoid large RF losses. The first method employs an additional ground layer between substrate and electrodes to shield the silicon from the RF signal [82, 83, 84]. This approach requires a multilayer fabrication process which can introduce additional difficulties in case of surface ion traps. In the second method, highly doped silicon is utilized as a material for electrodes of the trap chip [85, 86]. The drawback of this method is the applicability to only room-temperature setups due to the low electrical conductivity of doped silicon at cryogenic temperatures. Another method was proposed in our group [9] and was employed in these studies. It is based on the usage of intrinsic silicon substrate covered with gold and cooled down to $T \approx 10\,\mathrm{K}$. It was shown that from 25 K to 40 K free holes are freezing out and $\tan\delta$ goes down so the sufficient amount of RF voltage ($\sim 100\,\mathrm{V}$) can be applied

for ion trapping. Such trap designs exploit the benefits of a cryogenic environment and the possibility to use MEMS technology.

6.2 Fabrication of the silicon-based traps

In this section, general microfabrication steps of silicon-based surface ion traps will be covered. We performed several fabrication runs of trap chips with similar designs in collaboration with the team of J. Edlinger at the FH Vorarlberg (FHV) in Dornbirn and with Infineon Technologies AG in Villach.

During the first run, the team of J. Edlinger did the patterning of the silicon substrate and we applied the final steps of metalization. With these chips, we were capable to measure the heating rate of the ion trapped 150 µm above the surface and to detect pronounced light-induced charge effect of the silicon substrate.

In our second fabrication run our master student Gerald Stocker guided the fabrication processes at Infineon Technologies AG. All the necessary steps of the chip fabrication were performed there. With these chips, we characterized in details the charge generation effect and performed electrical studies of the silicon substrate in the presence of an external light sources at 10 K.

Fabrication at the FHV

For the fabrication in Vorarlberg, we used Topsil float zone silicon (very pure silicon) wafer with a thickness of 525 µm and a diameter of 100 mm. The resistivity of this wafer is specified to be larger than 5000 Ω cm.

The silicon wafer was spin coated with 2.4 µm of positive photoresist, as shown in Figure 6.1 (1). The next fabrication step was to irradiate the photoresist through a chromium mask with UV light. Then the photoresist was removed with a solvent as shown in Figure 6.1 (2)-(3). Deep reactive ion etching (DRIE) is used to pattern the gaps between the gold electrodes in the silicon wafer and is shown in Figure 6.1 (4). Detailed information about DRIE is presented in section 8.3. The described fabrication process creates 100 µm deep and 10 µm wide trenches which are tapered by ~ 2 µm. Finally the silicon wafer is cleaned from residual photoresist with O_2 plasma and a 2 µm layer of SiO_2 is created by wet thermal oxidation [87] as shown in Figure 6.1 (5)-(6). Then the wafer was covered on top with protective foil and diced into 52 chips.

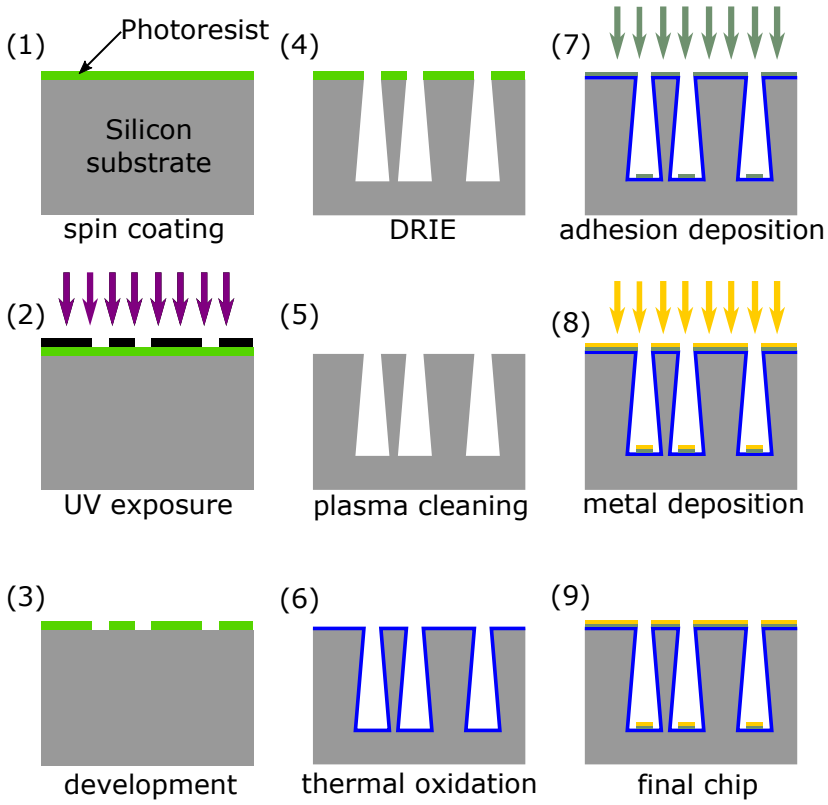


Figure 6.1: General steps of the trap fabrication performed in the Vorarlberg (1)-(6) and Innsbruck (7)-(9) facilities. Further details can be found in the main text.

The diced chips were finally sent to Innnsbruck's cleanroom for further fabrication steps:

1. Removing protective foil;
2. Cleaning the chip with detergent (Simple Green [a]);
3. Cleaning the chip with acetone and methanol in ultrasonic bath for 5 min in each solvent;
4. Drying the surface of the chip for 5 min with N_2 gas;
5. Mounting the chip in the evaporation chamber. Pump the chamber to pressure $< 5 \times 10^{-6}$ mbar;

[a] Simple Green, All-Purpose Cleaner

6. Evaporation of 2 nm of titanium adhesion layer (Figure 6.1 (7));

7. Evaporation of 200 nm of gold (Figure 6.1 (8));

8. Extraction of the completed trap chip from the chamber (Figure 6.1 (9)).

Fabrication at Infineon

At Infineon we used a 200 mm diameter wafer of p-Type silicon with high resistivity to decrease charge carriers in the silicon. Here, a wafer with a resistivity of more than 8000 Ω cm was selected.

The fabrication started with thermal oxidation of the silicon substrate. A 1.3 µm layer of SiO_2 is employed to create an insulating barrier between the gold layer and the silicon substrate. Also, the oxide layer is used as a hard mask for the upcoming lithography. The next steps include spin coating of SiO_2 layer with positive resist and patterning the topology of the trap on top of the chip by standard optical lithography.

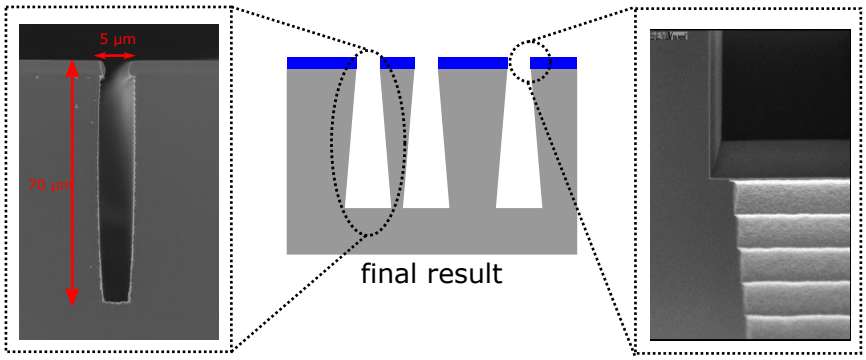


Figure 6.2: On the left side of the figure, the SEM picture of the trench in the silicon substrate, courtesy of Gerald Stocker. This trench does not have a tapered shape. But because of the pronounced undercut on top of the trench, the electrodes of the chip are separated after gold evaporation. On the right side of the figure, the scallop-like structure of the trench and pronounced undercut below the oxide layer are depicted.

An isotropic etch process with hydrofluoric acid (HF) was performed to expose silicon. The subsequent O_2 plasma cleaning removed from the chip surface the remaining parts of the photoresist. The described steps allow us to produce the on-chip hard mask with trap topology for the upcoming DRIE process. The final results of DRIE are scallop-like structure of the trench and pronounced undercut below the oxide; see Figure 6.2.

In the next step, tetraethyl orthosilicate (TEOS) was used in order to produce a silicon dioxide layer with very high conformity and excellent insulating properties. Low pressure chemical vapor deposition with TEOS requires ozone (O_3) as precursor during the reaction and to low the deposition temperature. The wafer is kept in a vacuum to prevent contaminations during the growth process. In Figure 6.3 (1) one can find that TEOS covers SiO_2 layer on top of the substrate as well as scallops on the trenches.

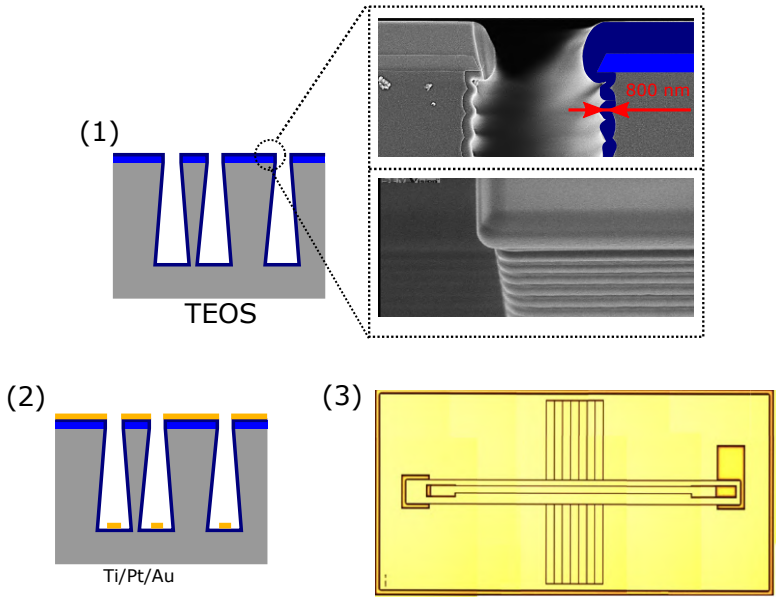


Figure 6.3: (1) Tetraethyl orthosilicate (TEOS) oxide deposition. (2) Titanium-Platinum-Gold metalization of the silicon substrate. (3) Picture of the final trap chip. Figure courtesy of Gerald Stocker.

The next step was to create conducting electrodes on top of the insulating layer. A titanium layer of 50 nm was used as an adhesion promoter. In order to prevent diffusion 100 nm of platinum was evaporated on top. The forthcoming step of 600 nm gold deposition formed the trap electrodes (Figure 6.3 (2)). The final step of wafer dicing (756 chips per wafer) finalized the chip production (Figure 6.3 (3)).

6.3 Design of the silicon traps

For both fabrication runs, we used one design of surface ion traps but scaled for different electrode-ion separation; see Figure 6.4. The general design of our silicon traps was named

after the Turkish prison "Yedikule" (YK), [44]. The YK trap design consists of seven segmented DC electrodes on each side of the RF rail which is separated by the central DC electrode; see Figure 6.4 (3). Seven DC electrodes allow to shuttle the ion along z axis. The mutually perpendicular x, y and z axes are aligned with trap axes as follows: The radial axes of the trap correspond to x and y coordinates and the axial direction of the trap is parallel to the z axis.

An asymmetric RF rail leads to a tilt in the principal radial trapping plane; see Figure 2.3. Such trap designs are called asymmetric. It allows one to achieve Doppler cooling in all motional axes with only one beam parallel to the chip surface.

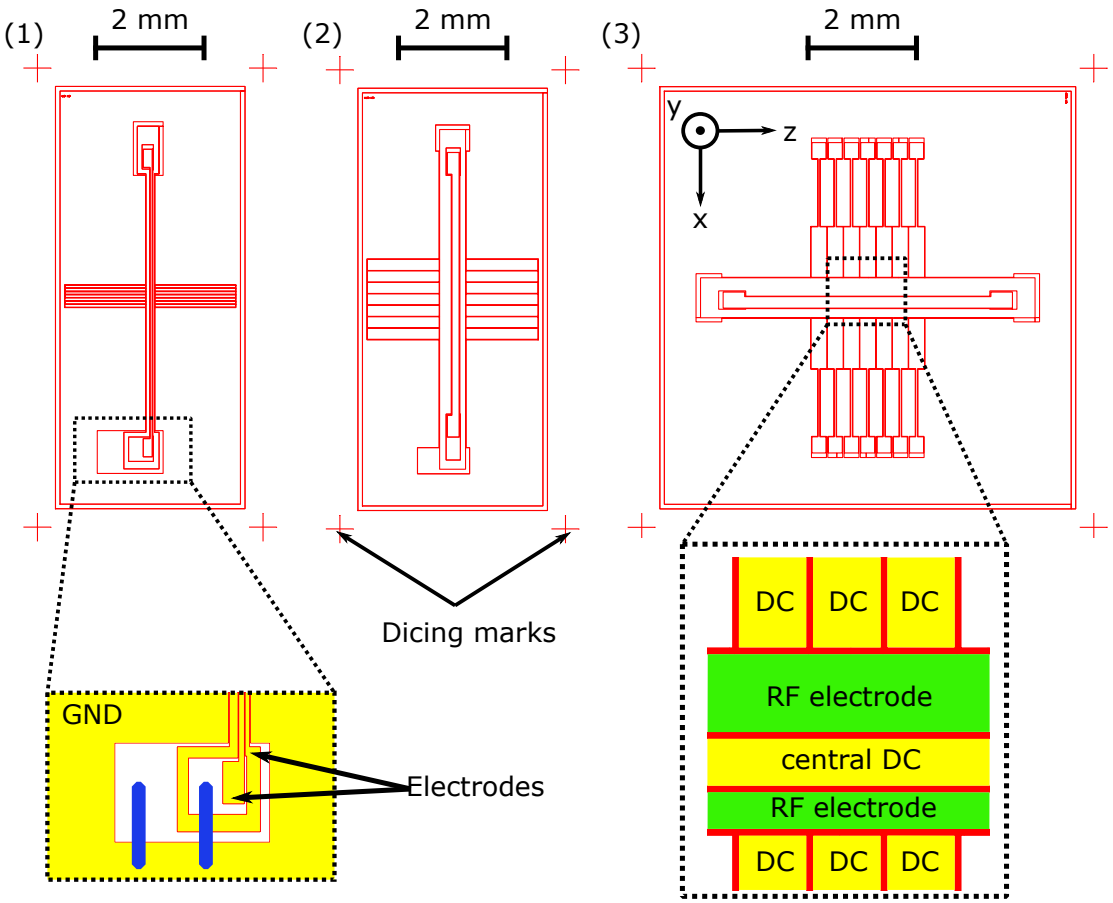


Figure 6.4: AutoCAD drawings of YK surface traps. (1) Design of the trap with 50 µm electrode-ion separation. In the insert, solution for the grounding of the bottom electrode inside of the trench. (2) Design of the trap with 150 µm electrode-ion separation. (3) Design of the trap with 230 µm electrode-ion separation. In the insert, layout of the trap electrodes.

Based on previous experience [9], a 10 µm gap between the electrodes was chosen for all the experiments in this thesis. To study the dependence of the heating rate versus electrode-ion separation and the charging effect (see section 6.5) we also designed additional chips with 5 µm and 15 µm gaps. It was possible to trap an ion in traps with 150 µm and 230 µm electrode-ion separation. Unfortunately, strong charge effect did not allow us to trap an ion in the trap with 50 µm electrode-ion separation as will be discussed in the section 6.6. All the chips have the capability to ground the bottom gold area of the trench; see Figure 6.4 (1). For that, the shape of the RF and central electrodes were modified in order to have additional space between them, this allows us to fit bonding wire.

This allows us to control the potential of this electrode and electrical bias it if necessary.

6.4 Characterization of the RF resonator

Ion trajectories in the trap are stable only at certain RF amplitudes. Those values can be determined by solving the Mathieu differential equations (2.2). For this the so called stability parameters $a \sim V_{\mathrm{DC}}$ and $q \sim V_{\mathrm{RF}}$ are usually introduced. The general requirement for stable operation conditions is $q \ll 1$. For our planar traps with 230 µm electrode-ion separation the requirements are even more strict: the q parameter should not be less than ~ 0.2 and should not exceed ~ 0.9 [44]. Additionally, the depth of the trap potential has to be more then 100 meV. All these criteria imply a lower limit for RF amplitudes of about $100\,\mathrm{V_{RMS}}$ and drive frequency ~ 20 MHz.

To achieve such high RF amplitudes we use a function generator combined with a lumped-element LC resonator [88]. The function generator creates an RF signal with typical amplitudes of about 10 V. An LC resonator inside of the cryostat steps up RF voltage signal. The LC resonator was chosen instead of an amplifier since it allows to the minimize the heat load of the cryostat. A detailed description of the circuit can be found in section 4.3. Here we will focus on the characteristics of the LC resonator.

The voltage step-up in the resonator is also called voltage gain G. In case of a matched circuit, G is given by the quality factor of the resonator Q, the inductor's resistance R and the impedance of the matched resonator Z_m:

$$G = \sqrt{\frac{R}{Z_m}}\,Q. \tag{6.2}$$

The measured quality factor of the LC resonator at resonance frequency $\omega_0 = 2\pi \times$

20.55 MHz for different temperatures is shown in Figure 6.5. It was measured with one of our silicon traps and with the aid of a impedance analyzer [b] and a cryostat temperature controller [c]. One can see that RF losses in the substrate are very high ($\tan\delta \approx 10^{-3}$) and the trap is not operable at temperatures of 310-165 K [81]. Between 165 K and roughly 30 K we observed a plateau of the quality factor. It appears due to the non-linear behavior of the material properties of the LC resonator circuit. Finally, at the transition temperature of 30 K, when charge carriers in the bulk of the substrate are frozen out, the quality factor goes to the maximum value of 870. Such a quality factor allows us to operate the trap chip in the cryogenic environment with minimal RF loss and heat load.

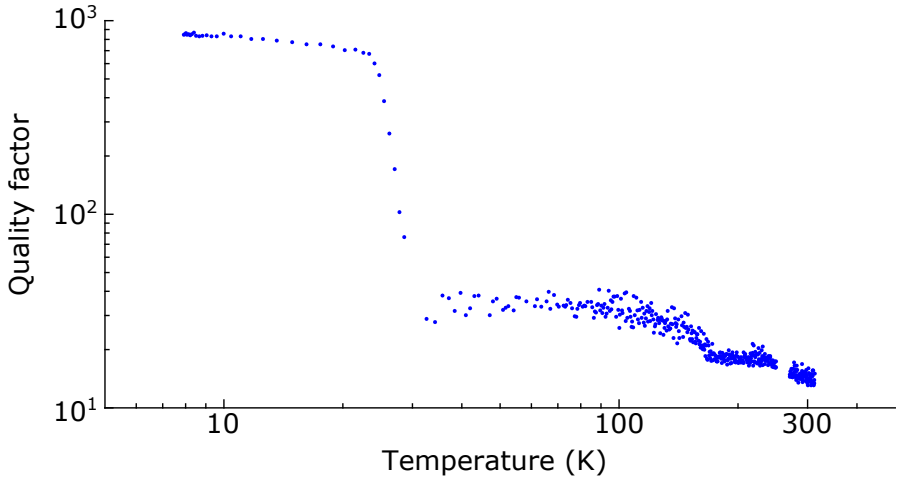


Figure 6.5: Quality factor Q of the LC circuit with a silicon trap for different temperatures. The resonance frequency is $\omega_0 = 2\pi \times 20.55$ MHz. Roughly at 25 K Q jumps up because charge carriers in the substrate are freezing out.

6.5 Light-induced charge carrier effect

As it was mentioned in the sections 6.1 and 6.4 the trap operation is impossible without freezing out charge carriers in the bulk of the silicon substrate. However, during the trap operation, laser light addressed to the ion can induce charge carriers in the silicon substrate. This is possible because there are large areas of uncovered silicon inside of the trenches. Also, the side walls of the trap chip are not coated, hence even the room light can penetrate

[b] VIA Bravo (AEA Technology)
[c] Cryo-con, model 24 Cryogenic Temperature Controller

to the substrate. The band-gap of silicon is 1.17 eV at 10 K [87]. As a result, all laser beams, which are used to manipulate $^{40}Ca^{+}$ ion have sufficient energy to induce charge carriers in the silicon; see Table 6.1. The light-induced effect of the charge generation has a profound negative influence on trap performance such as non-compensatable micromotion. The reduction of the trap size causes smaller electrode-ion separation. As a result laser beams have to be placed closer to the trap surface, and more laser light penetrates to the chip trenches. Hence, the discussed effects should in fact scale with the trap size.

Table 6.1: Wavelengths and corresponding energy of the laser beams, which are used to manipulate the $^{40}Ca^{+}$ ion. The band-gap of silicon is 1.17 eV at 10 K [87].

nm	eV	**Laser type**
377	3.3	Photoionisation
397	3.12	Doppler cooling
422	2.94	Photoionisation
729	1.7	Qubit
854	1.45	Repumping
866	1.43	Repumping

The study of the light-induced charge carrier effect in the remaining part of the thesis will be structured in the following way. The light-inducted charge carrier effect has been observed for the first time in the trap with 150 µm electrode ion separation, which was fabricated at Infineon; see section 6.6. Then we used the trap chip with $d = 230\,\mu m$ (fabricated at FHV) in order to confirm the observed effect, which was previously used in M. Niedermayr's Ph.D. research [44] and did not show signs of the light-induced charge carrier effect; see section 6.6. Afterwards, we used the trap chip with $d = 230\,\mu m$ (fabricated at Infineon) in order to minimize the charge carrier effect by means of grounding or biasing the substrate; see section 6.7.

6.6 Scaling down silicon surface ion traps

The first study of silicon based surface ion traps was realized by Michael Niedermayr [9]. It was shown that the ion trapped 230 µm above the trap surface experiences heating rates as small as $\Gamma_h = 0.33$ phonons/s at 1 MHz. In 2014 it was the lowest heating rate presented in any surface ion trap.

The goal of this work was to study how the anomalous heating rate [89] scales with the ion-to-electrode distance. With FH Vorarlberg we designed and fabricated traps with electrode-ion separation of 50 µm, 100 µm, 150 µm, 230 µm, 300 µm and 400 µm. In addition, trap designs with electrode-ion separation 50 µm, 100 µm, 150 µm have several options for gaps between electrodes.

Electrical tests of 150 µm traps

As a next step, we characterized trap with 150 mm electrode-ion separation fabricated in FH Vorarlberg; see section 6.2. This trap has 5 µm gaps in between electrodes and the gold plane at the bottom of the trenches is grounded. Linear gain and reflection coefficient of the RF circuit for different drive frequencies were measured at 10 K and are shown in Figure 6.6 (1). For this an impedance analyzer [d] was used to sweep over the input frequency and to monitor the reflected and transmitted signals.

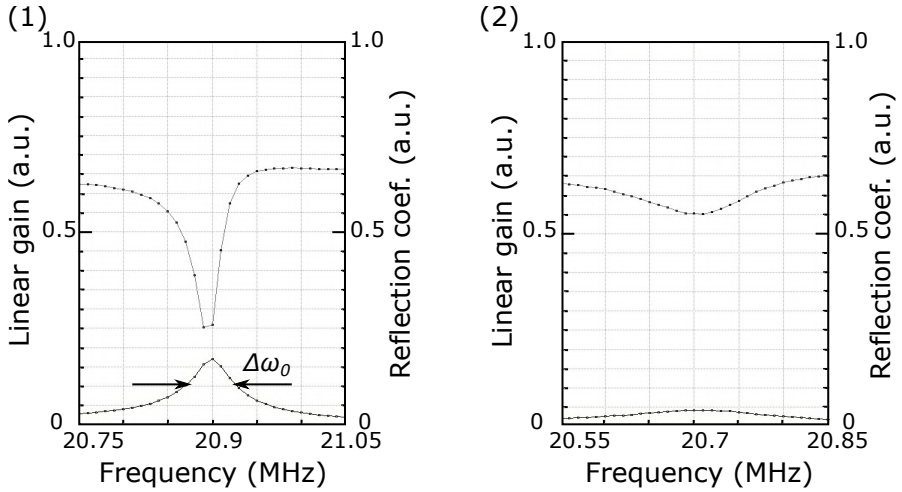


Figure 6.6: RF resonance for the trap with 150 µm electrode-ion separation. Linear gain and reflection coefficient as a function of the drive frequency at 10 K before (1) and after (2) breakdown.

From Figure 6.6 we found the resonance frequency ω_0 of $2\pi \times 20.9$ MHz and $\Delta\omega_0 \approx 2\pi \times 48$ kHz. Finally, the quality factor Q = 870 was calculated according to

$$Q = 2\frac{\omega_0}{\Delta\omega_0}. \tag{6.3}$$

[d] VIA Bravo (AEA Technology)

These parameters of the resonator allow us to achieve at least $V_{RF} = 76$ (see section 2.1) at $\omega_{RF} = 2\pi \times 20.9\,\text{MHz}$, required for stable operation. This RF voltage on the electrode corresponds to a signal on the capacitive divider of $V_{\text{cap.div.}} = 384\,\text{mV}$ 4.3.

With a function generator [e] connected to the LC resonator, we slowly increased the output voltage of the generator up to the required $V_{\text{cap.div.}} \approx 200\,\text{mV}$. During this procedure we observed electrical breakdown of one of the components of the resonator circuit. The signal of the capacitive divider suddenly jumped to 0 V. We repeated our electrical test of the resonator, presented in Figure 6.6 (2). One can see a clear shift in resonance frequency and decrease of Q factor almost to 0. We tried to reanimate the chip by heating it up to 250 K and cooling it back down to 10 K. This procedure should allow charge carriers to abandon the silicon substrate, but was not successful.

Another two attempts with the same trap chip design and wire bonding layout gave the same negative result. We observed electrical breakdown when V_{RF} reached the values of $\approx 40 - 50\,\text{V}$. We did not observe any damage of resonator components, bonding wires or visible defects on the gold-coated surface of the trap. Therefore, we infer that the observed breakdowns were due to damage either in the bulk of silicon or SiO_2. However a fourth chip was able to hold the voltage up to 80 V, which was enough to trap an ion.

Observation of the charging effect with the 150 µm trap

The pronounced light-induced charge generation effect was observed for the first time in traps with ion-surface separation of 150 µm. We observed variations of the ion fluorescence (see Figure 6.7) which we associated with the displacement of the ion from its position. The slow drift of the generated charge carriers in the bulk of the silicon leads to a displacement of the ion with respect to the laser beam. The charge carriers can be generated by the room light source used in the laboratory. We use lamp tubes [f] with color temperature of 4000 K. Light with this color temperature gives a broad continuous spectrum from 400 nm to 840 nm with few pronounced peaks of intensity [90] and therefore can generate charge carriers in silicon (see section 6.5 for details). The bottom CF160 window (see section 4.1) of our vacuum chamber has no coating and room light without attenuation penetrates inside the 4 K - stage. Scattered light hits side walls of the chip's trenches and induces charge carriers in the silicon substrate.

[e] Marconi signal generator 2024
[f] MASTER TL-D Super 80 38W/840 SLV/25

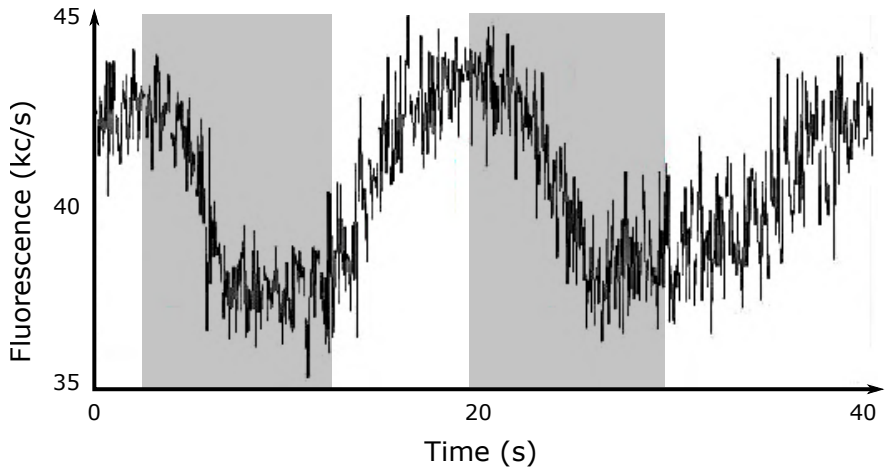


Figure 6.7: Ion's fluorescence oscillation caused by room light. Grayed region indicates time when room light was off.

The variations of the ion fluorescence caused by the room light are shown in Figure 6.7. Grayed regions in Figure 6.7 indicate the time when the room light source was switched off. When the room light was turned on we optimized experimental parameters to achieve the maximum of atomic fluorescence. We minimized micromotion and aligned all the necessary laser beams as well as PMT to the ion position. We assumed that all stray fields caused by the lamps dissipated or were in the equilibrium. When the room light was turned off we observed a slow process of charge carrier redistribution with characteristic relaxation time of around 5 s.

To further investigate the charging effect we used laser light pointed directly to the ion. For this, we used the laser beam with 729 nm wavelength with a power ~ 1 mW. We observed quantum jumps [18], as expected, but also a sudden leap of atomic fluorescence related to the ion displacement (Figure 6.8). After the laser light was switched off we observed roughly five times slower fluorescence level recovery than in the case of room light.

In addition, step-like recovery process was observed (Figure 6.9). Each step is about 15 kilocounts/s and occurred every 10-15 s till initial level of fluorescence was reached. The amount of steps varied from 1 to 3 depending on the intensity of the laser light. This effect was not observed in the case of the stray room light. We associate the appearance of multiple steps with the generation of charge carriers in the silicon when the laser light is applied. Therefore, steps indicate fluorescence recovery in (Figure 6.9) and are associated

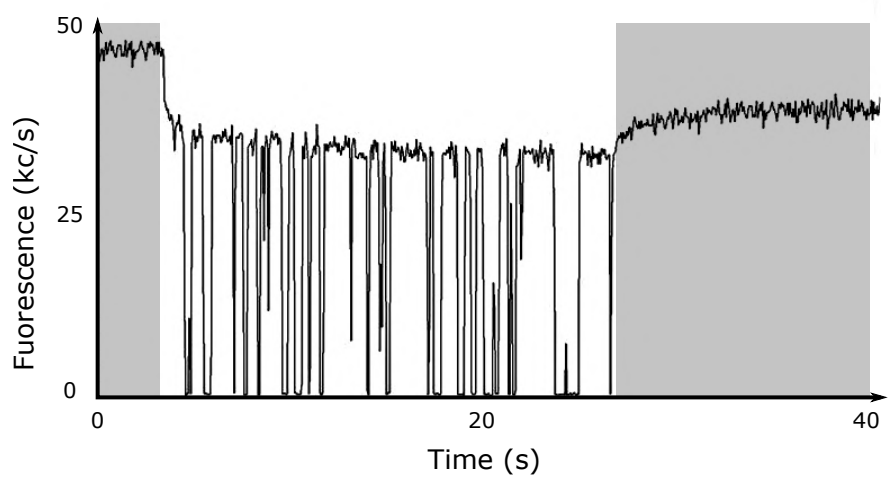


Figure 6.8: Detecting light-induced charging effects with laser beam. The laser beam with 729 nm wavelength was pointed directly on the ion. The grayed region in the plot shows the time period while laser is off. Quantum jumps are observed when laser light is turned on.

with slow dissipation of charge carriers in the bulk of the silicon substrate.

To examine the role of the charge generation effect in the heating rate we measured Γ_{h} using the 729 nm laser tuned to the $S_{1/2} \leftrightarrow D_{5/2}$ quadrupole transition. For this we prepared the ion in the ground state of its axial mode by Doppler and subsequent sideband laser cooling. Unfortunately, the cooling process was unstable due to the drift of the micromotion caused by the ion displacement. We observed the drift of the Rabi flop amplitude on the micromotion sideband over the short period of time of about a minute. We managed to compensate the micromotion up to the flopping time $\tau_{\pi}^{\mathrm{MM}} \approx 300\,\mathrm{ms}$ while the flopping time on the main carrier was $\tau_{\pi}^{\mathrm{C}} \approx 10\,\mathrm{ms}$ (Figure 6.10). But after 20 s of waiting, the flopping time was degrading to values less then $\tau_{\pi}^{\mathrm{MM}} \approx 250\,\mathrm{ms}$ and after 1200 s waiting time Rabi oscillations came back to the value before micromotion compensation. Such behavior indicates the shift of the ion position caused by the generation of charge carriers and their further redistribution in the trap. Nonetheless, it was possible to make a preliminary measurement of the heating rate $\Gamma_{\mathrm{h}} \approx 3.15\,\mathrm{phonons/s}$ at 1 MHz axial frequency. With this trap it was not possible to achieve optimal laser cooling because of the micromotion drift. Eventually, we tried to increase the RF voltage to see if this would affect charge carrier generation but the trap had an electrical failure.

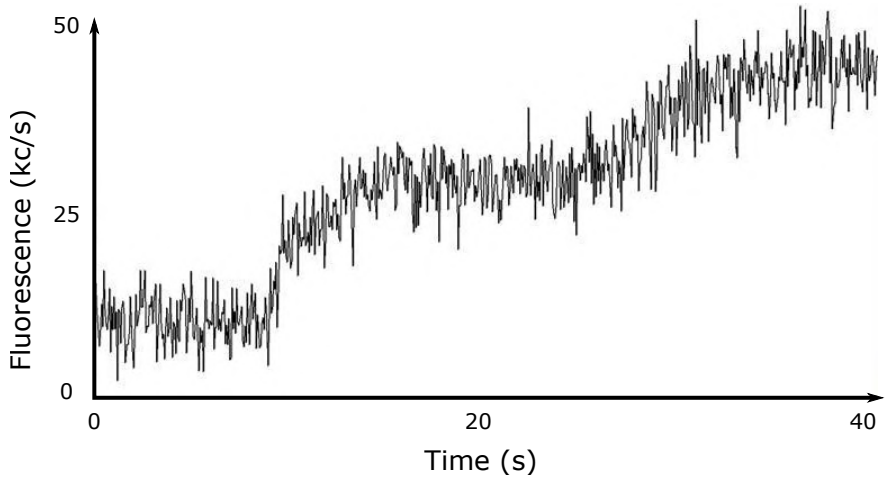


Figure 6.9: Recovery of atomic fluorescence after 1 mW of 729 nm laser light, which was used to address the ion. The fluorescence recovery process has a pronounced step function.

Second run of the 230 µm trap

In a previous study [9] of a trap with 230 µm electrode-ion separation, produced at FH Vorarlberg, the light-induced charge generation effect was not observed. Both studies [9] and [44] focused on measurements of heating rates and on obtaining statistics of operability for different traps with the same design. The charging effect could have gone unnoticed in three studies. Therefore we decided to examine this trap again in order to find any sign of the charge generation.

It is important to mention a few aspects of this study [44] relevant for the further discussion. First, the heating rates measured for the same trap geometry vary in a broad range [9]. The largest difference was detected for different wafers of the same design as can be seen in Table 6.2. Second, the lowest heating rate was $0.33(4)$ phonons/s measured for trap 5. After measurements performed in the experiment presented in the article [9], the trap with the smallest heating rate was stored in the cleanroom for 3 years and then was mounted again in the cryostat. After storage, this trap showed the heating rate $\Gamma_{\mathrm{h}} = 2.20(4)$ phonons/s, which is one order of magnitude higher than before. We attribute the observed heating rate to the surface contamination or surface degradation of the chip.

During my Ph.D. work, 230 µm traps were operated using tightly focused laser beams with 729 nm wavelength. The beam had a waist of 30 µm and the laser was tuned to the $S_{1/2} \leftrightarrow D_{5/2}$ qubit transition. In the first test, the laser beam was centered on the ion. We observed quantum jumps and well-defined fluorescence steps of 5 kilocounts/s. For

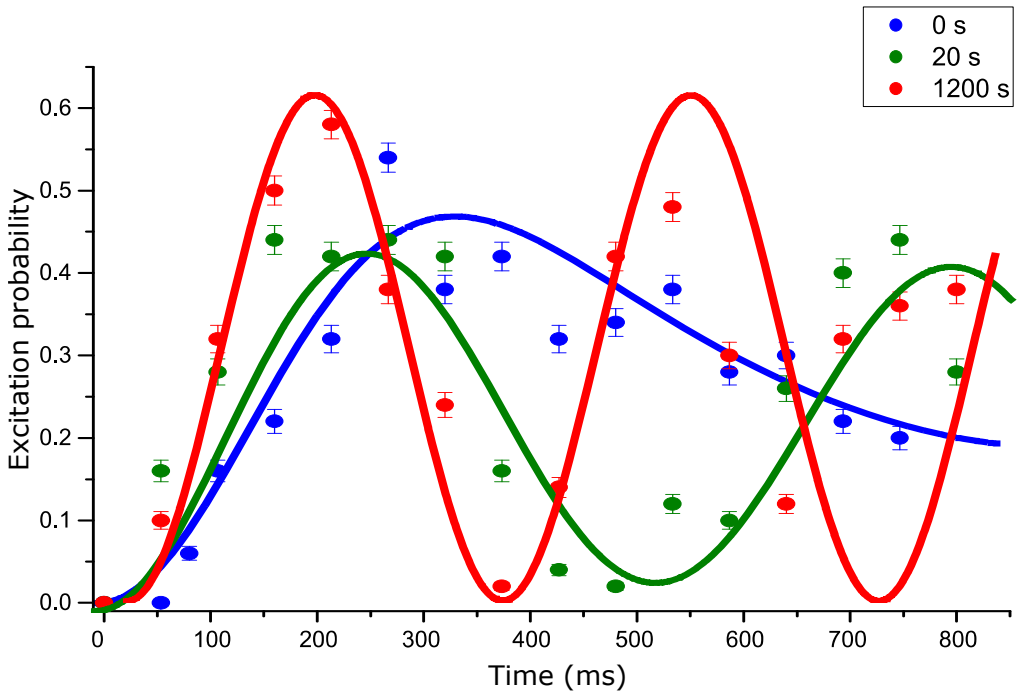


Figure 6.10: Drift of the Rabi flop on the micromotion sideband over time for 150 µm trap. Solid lines are a fit to the experimental data (dots). Blue line and dots depict the flop on the micromotion sideband directly after voltage compensation. Green line and dots are obtained after 20 s waiting time. Red line and dots are obtained after 1200 s waiting time. The displayed error bars represent 1-σ fluctuations from detection shot noise.

comparison, fluorescence steps in the case of the 150 µm trap were about 10 kilocounts/s (Figure 6.8) for the same laser power. Such a difference in the fluorescence jumps is likely caused by the fact that the laser beam was directed further away from the surface and therefore less amount of light penetrated to the the bulk of the silicon substrate. In the second test, we placed the laser beam directly below the ion's position in order to increase the amount of light penetrating into the trenches. We used 729 nm laser light with a power $\sim$ 1.4 mW. We observed a fluorescence step of 10 kilocounts/s (Figure 6.11 (2)), in contrast to the previous case (Figure 6.11 (1)). When the laser light was switched off, a slow recovery process with two small steps has been observed. In the third test, the laser beam was placed on the surface directly below the ion and horizontally moved 200 µm away from the ion. We observed even bigger fluorescence jumps of 15 kilocounts/s followed by two recovery steps, when the laser light was switched off. All three tests show the pronounced response of the ion's fluorescence on the silicon substrate irradiated with

Table 6.2: Heating rates of six traps, all of the same YK design [44], with an ion-electrode separation of 230 µm. The numbers in brackets indicate error bars. The error bar for trap 1 was calculated using the results over six weeks of measurements and represents the standard deviation of the mean. The error bars for the traps 2-6 indicate the uncertainty in a single heating-rate measurement and represent standard deviation. The table was taken from the Ph.D. thesis of M. Niedermayer [44].

Trap	**Wafer**	**Heating rate** (phonons/s)	**Axial freq.** (MHz)
1	1	0.6(2)	1.069
2	1	3.3(2)	1.059
3	1	0.96(7)	1.069
4	1	0.95(7)	1.045
5	1	0.33(4)	1.066
6	2	21.5(8)	1.073

the laser light.

Additionally, we tested how strong the ion is influenced by collisions with background gases. For this we measured the dark lifetime of the ion. The idea of the experiment is the following: After optimizing Doppler cooling, the 397 nm laser light was switched off and the ion was left in the trap without cooling for some waiting time. Then we turned on the laser and checked whether the ion escaped from the trap. If the ion is still trapped we increase the waiting time, if not we repeat the last waiting time another three times. We measured a dark lifetime of 300 s which is a low result compare to previously measured in our setup [44].

We observed a charge effect induced by 397 nm laser light during the dark life time measurement. When the laser light was switched on we observed displacement in the axial direction of the ion from the initial position. After switching on the light, in Figure 6.12 we observe the decrease of the ion fluorescence before it goes up and then saturates. The reason for this could be more energetic photons of laser light (Table 6.1) which cause more drifting charge carriers. Nonetheless, we have not observed pronounced steps during the recovery of fluorescence as was reported before; see Figure 6.9.

We also tested the influence of different light sources on the RF resonator while DC electrodes are grounded or connected to filters outside of the cryostat (see Figure 6.13). For this, we checked the behavior of the voltage on the capacitive divider (see section 6.4)

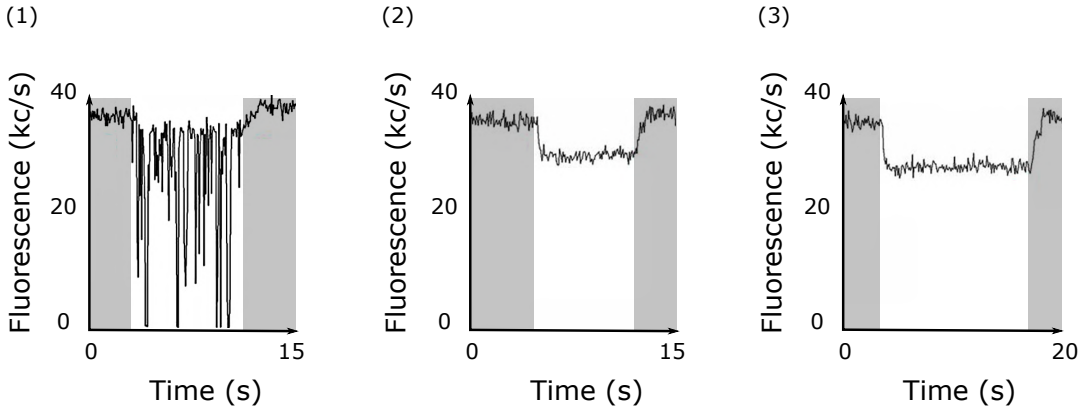


Figure 6.11: Charging effect observed in the 230 µm trap induced by the laser light with wavelength 729 nm. The grayed region indicates the absence of 729 nm laser light. (1) Laser beam was centered on the ion.(2) Laser beam directly below the ion's position. (3) Laser beam was placed on the surface directly below the ion and horizontally moved 200 µm away from the ion.

while irradiating the silicon substrate with laser light. We did not observe a correlation between power or position of the different light sources and the voltage on the capacitive divider.

In summary, we observed light-induced charge generation effect in the traps with 150 µm (Infineon fabrication) and 230 µm (FH Vorarlberg fabrication) electrode-ion separation. The induced charges can be generated by any light source with the wavelength less than 1060 nm and displace an ion from the original position. As a result the charge effect causes the ion to drift and change micromotion parameters which is impossible to compensate with applying additional DC voltages.

In the ion trap with electrode-ion separation of 150 µm the lasers were placed closer to the silicon substrate: Hence more pronounced charge carrier effects have been observed. With such an ion trap, we measured the heating rate $\Gamma_h \approx 3.15$ phonons/s at 1 MHz axial frequency before electrical failure of the trap chip. However, a trap with 230 µm electrode-ion separation showed less strong charge effects and more stable operation. Therefore, traps with large electrode-ion separation were chosen for further studies of the light-induced charge generation effect.

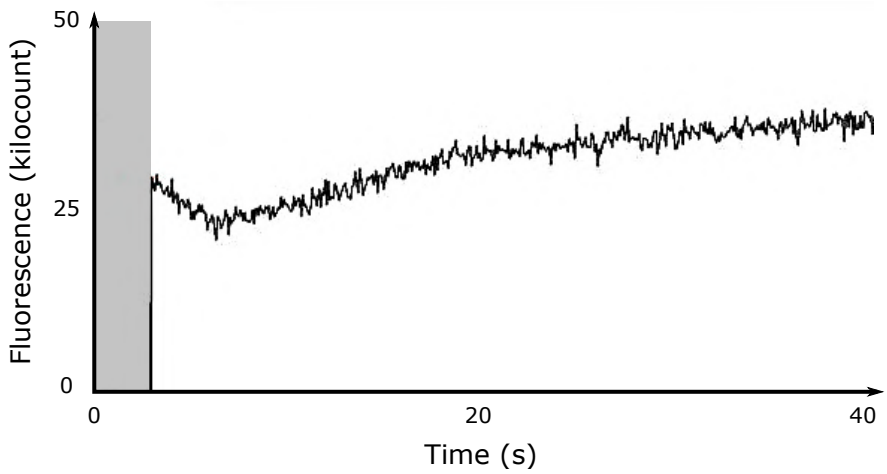


Figure 6.12: Charging effect induced by the 397 nm laser light. The grayed region region indicates the absence of the 397 nm laser light.

6.7 Study of the light-induced charge generation effect

The production of the charge carriers in silicon induced by different light sources is a major obstacle (6.6) for scaling down silicon-based surface ion traps. Our goal was to better understand and reduce the charge generation effect in the trap substrate. We choose the same trap design with 230 µm electrode-ion separation (see section 6.3) used for the traps discussed earlier in section 6.6. The trap chip was produced at Infineon; see section 6.2. For the present study the chip size was reduced from 1×1 cm to 0.8×0.7 cm. This modification was necessary to fulfill the requirements of the well-established fabrication processes at Infineon. The modified trap design has an advantage of additional space between the copper carrier and the trap chip which was used to introduce electrodes for biasing silicon substrate.

With electrodes connected to the substrate, we can significantly improve grounding of the silicon. Also, additional DC bias voltages can be applied to the substrate. It can redistribute the charge carriers and hence reduce their effect on the ion. With such a setup, it is possible to measure the electrical response of the silicon on the light which can characterize the charge effect quantitatively.

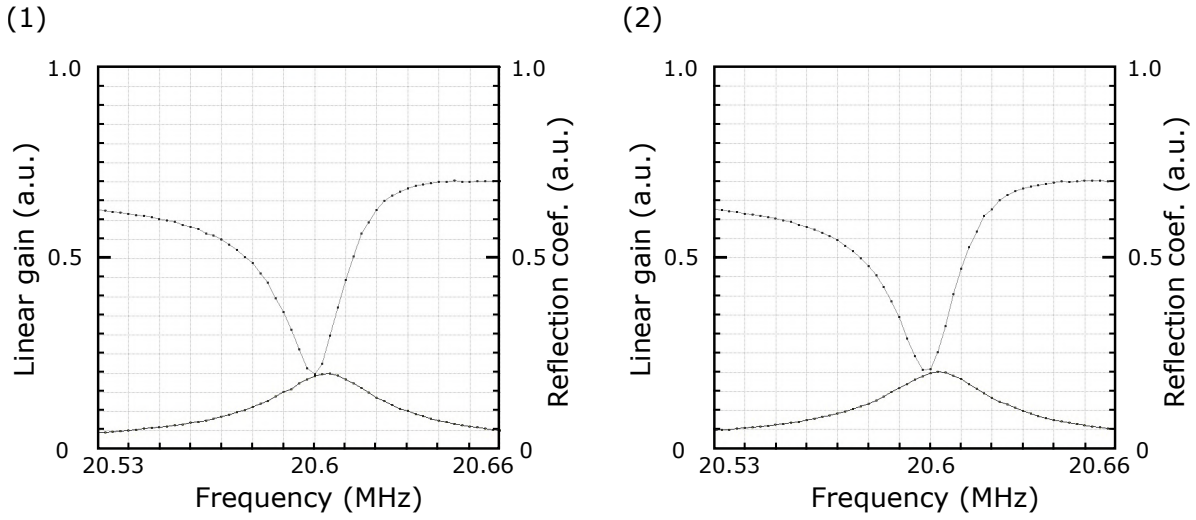


Figure 6.13: RF resonance for the trap with 230 µm electrode-ion separation. Linear gain and reflection coefficient as a function of drive frequency at 10 K when all DC electrodes of the trap are connected to the main ground (1) and when DC electrodes are connected to filters outside of the cryostat (2).

Tests of the $d = 230\,\mu\text{m}$ trap with not grounded silicon substrate

As a reference test, we used the trap chip (230 µm electrode-ion separation) produced at the Infineon without electrodes connected to the silicon substrate. This necessary in order to exclude differences in the fabrication at FHV and at Infineon. The design of this trap chip had a mistake. Namely, one of the DC electrodes was shorted to the ground plane of the chip. To resolve the issue we cut part of the electrode placed far from the trapping with sharp blade. Then we verified that the trap is operable by performing electrical and optical inspections. The surface of gold below the ion was in perfect conditions for heating rate measurements. However, this defect exposed a large silicon area to the light and therefore restricted the working area of the chip.

Several tests have been performed with this trap chip involving different light sources. In the first test we used room light [91, 90] to induce charges in the substrate. We detected 0.2 µm displacement of the ion in the axial direction with fluorescence step of about 3 kilocounts/s (Figure 6.14 (1)). This result was reproducible and comparable with 5 kilocounts/s shift observed on the trap fabricated at FH Vorarlberg and discussed in section 6.6.

During our second attempt we made series of tests of generating charge carriers with

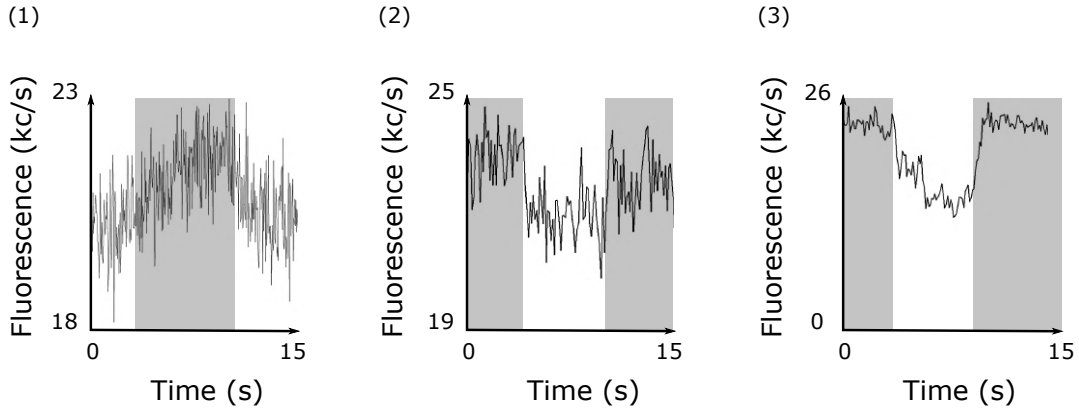


Figure 6.14: Detecting of the light-induced charge carrier generation for trap produced at Infineon with not grounded silicon substrate. Grayed region region indicates absence of the light. (1) Ion displacement caused by room light. (2) Ion displacement caused by LED pointed towards front gold surface of the trap. (3) Ion displacement caused by LED pointed towards edge of the chip, light hits uncoated silicon substrate.

white LED (Light-emitting diode) sources. We used LED light source [92] with a maximum optical output power of $\approx 2\,\mathrm{W}$ and a broad spectrum ranging from approximately 380 nm to 780 nm [93]. During these tests room light was always off. Figure 6.14 (2) shows the result of the measurements. The LED source was placed towards the gold surface of the chip so only silicon inside of the chip trenches was exposed to the light. We detected 2 kilocounts/s fluorescence shift and an ion displacement in the axial direction of 6.5 µm [g]. Afterwards, we aligned the LED in front of one of the side optical viewports (see Figure 4.2) so light hits the lateral section of the chip which is parallel to the RF rails. This part of the chip surface is not coated with gold but covered with a few nm of native silicon oxide. The result of this test is shown in Figure 6.14 (3). We observed 13 µm displacement of the ion in the axial direction and a fluorescence shift of more than 10 kilocounts/s on the PMT (Figure 6.14 (3)). From these tests, we conclude that the larger silicon surface area exposed to the light causes the larger displacement of the ion that was observed, due to the stronger charge carrier effect.

Finally a drift of the Rabi flop time on the micromotional sideband has been measured with a 729 nm laser light; see Figure 6.15. We used 3 DC electrodes on each side of the RF electrode and the central DC electrode to compensate the micromotion. The Rabi flop time

[g] The displacement of the ion was measured using python program written by R. Assouly (former group intern). This software calculates relative shift of the ion from the CCD camera data.

on the carrier transition was measured to $\tau_\pi^C \approx 7\,\text{ms}$. The longest flop time achieved after this process was $\tau_\pi^{MM} \approx 60\,\text{ms}$ and is depicted in Figure 6.15 with blue line and squares. In fact, the flopping time was not constant and was drifting in time. After 60 s and 240 s of waiting we probed the flopping time of 80 ms and 110 ms respectively. After 480 s of waiting and micromotion compensation we observed the decrease of the flopping time and measured the flopping time of 90 ms. The latter is shown in Figure 6.15 with red line and squares. The observed drift in the flopping time indicates that trapped charge carriers in the bulk of the silicon substrate can't escape the substrate and could stay inside for an extended period of time.

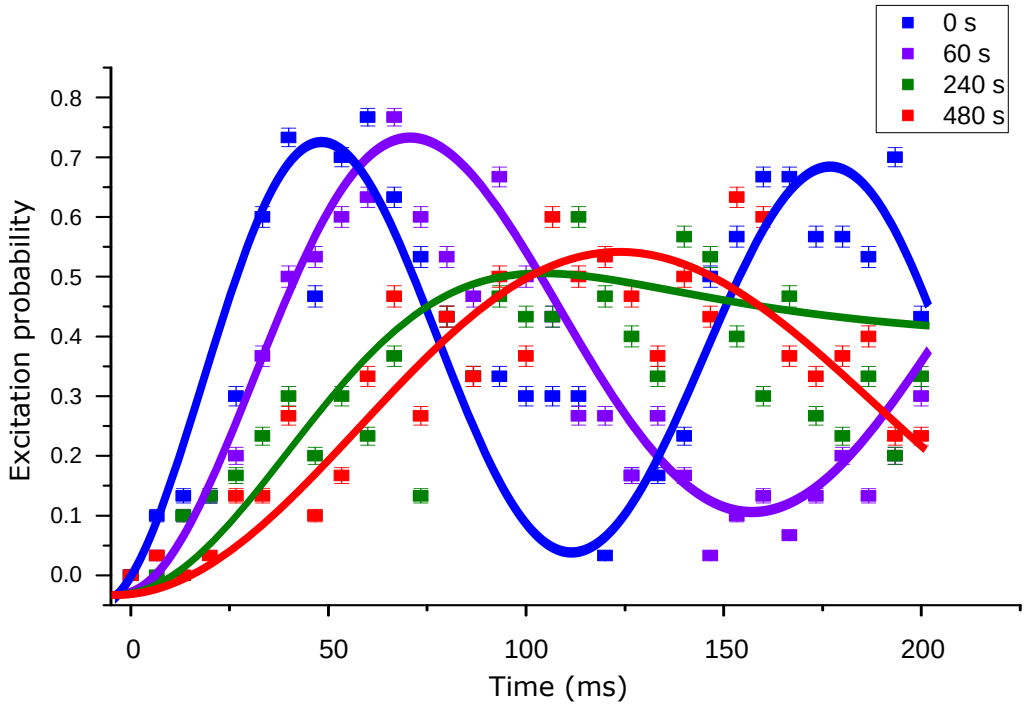


Figure 6.15: Drift of the Rabi flop on the micromotion sideband over time for 230 µm trap. Solid lines are a fit of experimental data (squares). Blue line and squares depict flop on micromotion sideband directly after a micromotion compensation procedure. Purple line and squares are obtained after 60 s of waiting. Green line and squares are obtained after 240 s of waiting. Red line and squares are obtained after 480 s of waiting. The displayed error bars represent 1-σ fluctuations from detection shot noise.

We made also several attempts to measure the heating rate of the ion using the resolved sideband ratio method (see section 3). First measurements gave the value of

$\Gamma_h = 133(24)$ phonons/s for 1 MHz axial frequency, which is two orders of magnitude higher than the heating rate measured with the FHV chip; see Table 6.2. After 5 hours we repeated the measurement and observed $\Gamma_h = 243(20)$ phonons/s. In both measurements it was not possible to cool the ion down to the ground state, only to a value of 0.2 phonons. The origin of the fluctuations of Γ_h as well as the relation between heating rate and the charge generation effects remain unclear. We think that higher heating rates should originate on the surface of the trap because these measurements were done after mitigating all technical noise source (see section 5).

In conclusion, we detected a light-induced charge carrier generation effect in the 230 µm trap produced by Infineon. The drop in the fluorescence of the ion induced by room light, 729 nm and 397 nm laser lights were of similar amplitude. Tests with LED lights source showed direct a correlation between the size of the exposed surface area of the silicon substrate and the charge generation. We detected two orders of magnitude higher heating rate for our trap than typical heating rate values for silicon traps with similar size [9, 44]. This behavior is not understood so far. The drift of the micromotion flopping time shows that charge carriers could stay inside for of the silicon extended period of time and interfere with the experimental processes.

Tests of the $d = 230\,\mu m$ trap with grounded silicon substrate

Our next goals were to understand and to mitigate light-induced charger generation effect. For this, we used trap chips from the same wafer as in the section 6.7 but with grounded silicon substrate and biased with DC voltage (section 6.7). These steps should compensate stray fields and redistribute charge carriers as well as help to electrically characterize the light-induced effect.

One of the steps of micro-fabrication of the silicon trap chips is thermal oxidation (see section 6.2 for details). During this process the whole wafer is placed in a furnace where an oxide layer of approximately 1.3 µm is grown. Then the wafer is diced into chips. As a result side walls of the chip have thinner layer of ≈ 1 nm of native oxide caused by direct exposure of the air to the silicon [94]. To contact the electrodes electrically we scratched this thin layer from two of the side walls of the chip with a sharp diamond scraper. Directly after this step we applied electrically conductive silver-filled epoxy EPO-TEC H20E [95] on all four sides of the chip to connect the substrate to the copper carriers which defines the main ground. To cure the epoxy we hold it at 120 C for 15 minutes. The resistance across

the substrate was 1.5 MΩ with untouched native oxide and 800 kΩ [h] after its removing. For these measurements we used standard multimeter probes on bare silicon.

After we cooled down the trap, we observed that the RF voltage on the trap electrode was drifting over the day. The RF voltage on the trap electrode is monitored with the voltage on the capacitive divider; see section 4.3. In the morning it was usually around 720 mV [i] and in the evening around 688 mV for the same amount of input power. The electrical properties of the RF resonator were recorded after the first cooling down and are shown in Figure 6.16 (1). The cryostat was warmed up to 80 K and cooled down to the base temperature. We measured a drop in the linear gain of the resonator from 0.14 to 0.055 (see Figure 6.16 (2)). Also we observed that after some certain input power on the resonator, the voltage on the capacitive divider went to a plateau. This could indicate that part of the input power is dissipated in the trap chip. We did not observe such a behavior in previous traps. We attribute the appearance of the plateau to the presence of the defects in the insulating layer which should lead to small conducting channels from the gold layer to the silicon surface. Overall such resonator behavior creates a significant problem for the trap operation. We were not able to apply the necessary RF voltage for ion trapping. However, after the third cooling cycle, the resonance properties became better (see Figure 6.16 (3)). Namely, the linear gain of the resonator was raised up to the 0.069. It was enough to apply sufficient RF voltage for ion trapping. We managed to cool the ion to its ground state, down to an initial state with 0.02 phonons. We did not observe micromotion drift at that time. However, the heating rate was strongly fluctuating over 2 hours from 129(12) phonons/s to 98(14) phonons/s. Unfortunately, the trap resonance degraded to the plateauing value of 620 mV on the capacitive divider so it was possible to load only clouds of ions. We decided to swap the trap and modify electrical grounding of the chip.

Tests of the $d = 230\,\mu m$ trap with biased silicon substrate

At first, we mounted the chip on two $10 \times 4\,mm^2$ Kapton stripes placed on each side of the chip [96]. The area between the Kapton stripes on the backside of the chip was coated with a thin layer of heat-conducting grease [97] which provided thermal connection between

[h] The calculated resistance of the chip from one side to another side was 200 kΩ. It was calculated using the resistivity of the substrate of 8000 Ω cm.

[i] The ration between the voltage on the capacitive divider and the RF voltage on the trap electrode is 400.

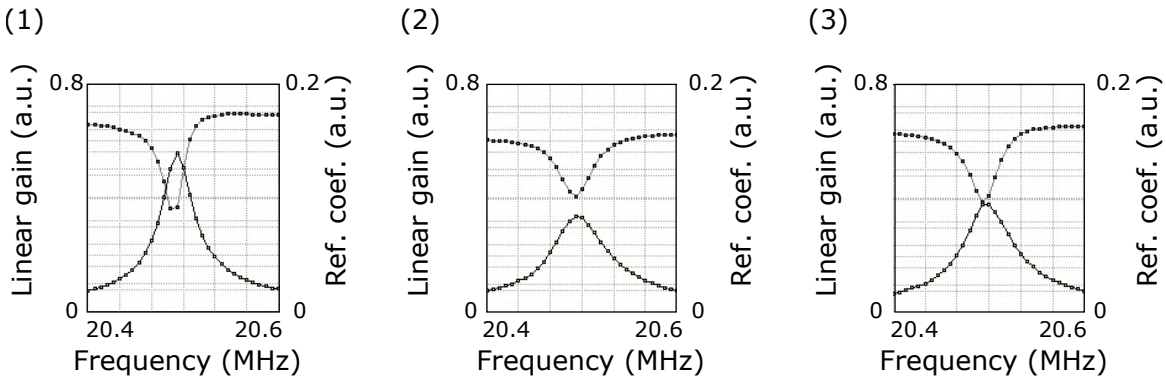


Figure 6.16: behavior of RF resonator over time. (1) First cooling cycle, linear gain is 0.14 and reflection coefficient is 77.9. (2) Second cooling cycle, linear gain is 0.055 and reflection coefficient is 73.2. (3) Third cooling cycle, linear gain is 0.069 and reflection coefficient is 75.4.

the trap and the copper carrier. Titanium clamps were used to hold the chip on the copper carrier (Figure 6.17). The clamps were fixed to the copper carrier by brass screws.

The side walls of the substrate were scratched with a diamond marker in order to remove native oxide and were covered with silver-filled epoxy [95] providing electrical contact for the two copper wires (1 cm length and 1 mm diameter). From one side the copper wire was glued with the silver-filled epoxy to the silicon substrate and from another side it was attached (with the silver-filled epoxy) to the DC channel of the PCB. Then epoxy was cured by keeping it at 120 C for 30 minutes. To have an ability to use the 4-point probes method we connected additional gold wire bonds from the PCB to the wire going to the substrate.

We measured the temperature dependence of the resistance of the substrate while cooling down the cryostat. It was rising linearly with temperature from 2.4 MΩ to 120 GΩ in the temperature range of $300-100$ K. Below ≈ 100 K resistance stopped rising because the multimeter achieved its maximum measuring range limited by 120 GΩ. During the measurement we switched off all light sources to avoid the influence of light-induced charge carriers. However, we switched on the room lights intentionally at temperature $T = 8, 70, 120, 180$ K. In each instance we observed a reduction of the resistance across the substrate to $R = 40$ MΩ.

As a next step, the silicon substrate of the chip was connected to the ground. The Rabi flopping on the micromotion sideband was measured for different waiting time (Fig-

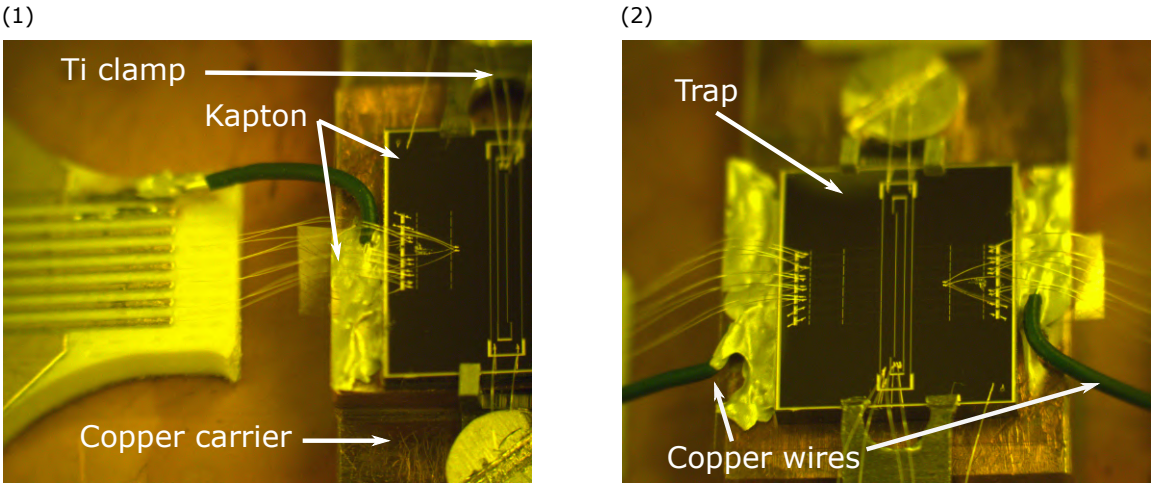


Figure 6.17: Mounting and contacting of the Infineon trap chip with DC biasing of the substrate. Additional connections were established between the silicon substrate and the channels of the PCB board. (1) Side view of the chip fixed with titanium clamps to the copper carrier and electrically decoupled from the ground with Kapton stripes. (2) The substrate of the trap is electrically connected on both sides of the chip to dedicated traces on the DC filter board.

ure 6.18). The flopping time of the micromotion sideband directly after the compensation of stray fields was $\tau_\pi^{\mathrm{MM}} \approx 70\,\mathrm{ms}$, the flopping time on the main carrier was $\tau_\pi^{\mathrm{C}} \approx 7\,\mathrm{ms}$. After 45 minutes of waiting, Rabi flop on micromotion sideband tuned out to be the same $\tau_\pi^{\mathrm{MM}} \approx 70\,\mathrm{ms}$ (Figure 6.18). During both measurements and during the waiting time between them the ambient light sources were not changed. Compared with traps whose substrates were not electrically contacted (Figure 6.10, Figure 6.15) this is a significant improvement in the stability of micromotion. However, it was not possible to achieve flopping times on micromotion sidebands bigger than $\tau_\pi^{\mathrm{MM}} \approx 70\,\mathrm{ms}$, usually it is possible to compensate up to $\sim 300\,\mathrm{ms}$. Additionally, we disconnected the silicon substrate from the ground to let it float, and observed a drift of the flopping time. We conclude that the grounding of silicon substrate reduces the number of charge carriers in the bulk of silicon but does not completely solve the issue with light-induced charge carrier effect.

In fact, we again observed a pronounced light-induced effect (see in Figure 6.19). We detuned the 729 nm laser light far from the $S_{1/2} \leftrightarrow D_{5/2}$ quadrupole transition to avoid quantum jumps. This light beam was centered on the ion, 230 µm away from the trap surface. At the laser power of 1 mW we did not observe any drifts in the ion fluorescence.

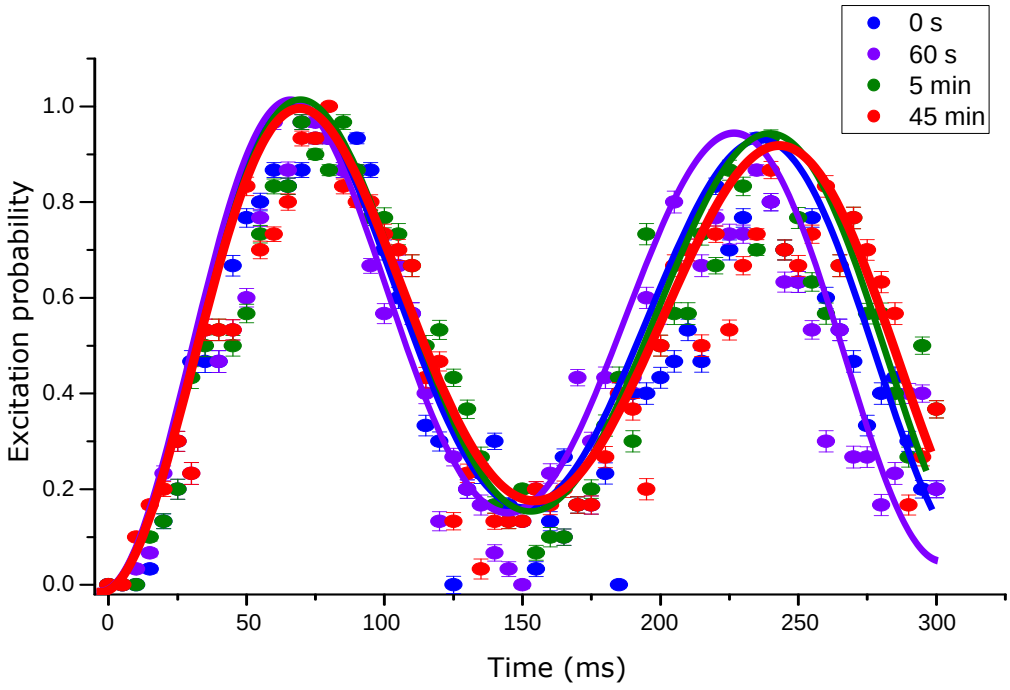


Figure 6.18: Drift of the Rabi flop on the micromotion sideband over time for 230 µm trap fabricated at Infineon. Solid lines are a fits of experimental data (dots). Blue line and dots show flopping on the micromotion sideband directly after voltage compensation. Purple line and dots are obtained after 60 s of waiting time. Green line and dots are obtained after 5 minutes of waiting. Red line and dots are obtained after 45 minutes of waiting time. The displayed error bars represent 1-σ fluctuations from detection shot noise.

Therefore we increased the laser power until we observed pronounced step in the ion fluorescence shown in Figure 6.19. This happened at the laser power of 12 mW, which is a significant improvement compared to previous studies (see section 6.7). A similar effect (fabricated at FHV) was previously observed with a similar trap chip (see Figure 6.11) at much lower laser power of $\sim$ 1.4 mW.

Our next step was to apply a DC bias to the substrate. Figure 6.20 (1) shows the electrical scheme used to bias the silicon substrate. A low-noise voltage source [j] was connected in between the gold surface of the trap and the silicon substrate (see Figure 6.20 (2)). The gold ground area of the chip (see Figure 6.4 (3)) placed around all DC and RF electrodes was connected to the main ground of the PCB and was connected with gold bonding wires

[j] ISEG, EHS F205x-F-K1

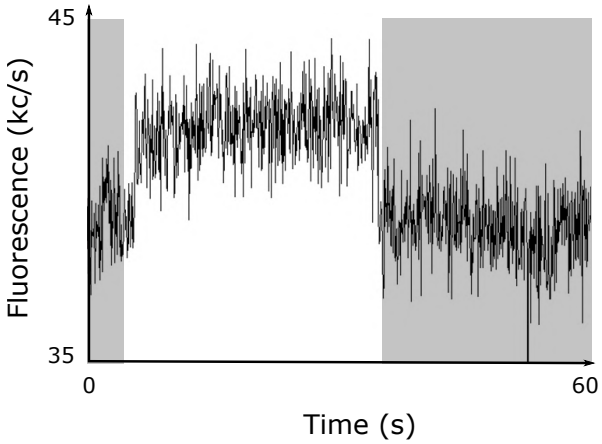


Figure 6.19: Detected ion fluorescence jumps induced by the light irradiating the trap with 230 µm electrode-ion separation (fabricated at Infineon). 729 nm laser beam with power 12 mW aligned directly on the ion. Frequency was tuned far from them $S_{1/2} \leftrightarrow D_{5/2}$ quadrupole transition to avoid quantum jumps. The grayed region indicates an absence of the 729 nm laser light. Errors bars are attributed to Shot noise.

to the same low-noise voltage source. The multimeter [k] was connected in parallel to the substrate to measure the voltage drop V_c through the substrate depicted as resistance R_t in Figure 6.20 (1). A second multimeter [l] was measuring the voltage drop across a resistance $R_c = 0.9152\,\mathrm{k}\Omega$ to determine the current in the circuit.

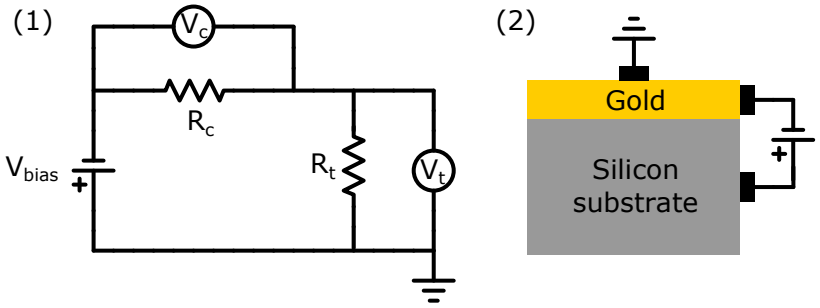


Figure 6.20: (1) Electrical scheme used to bias the silicon substrate. The silicon substrate is depicted as R_t. (2) The electrical connection of the silicon to the low-noise voltage source.

To find any correlation between the bias voltage applied to the substrate and the noise experienced by the ion we performed a series of heating rate measurements over the period

[k] Fluke 116
[l] KEYSIGHT U1251B

of three days. The idea is the following. The voltage applied between the gold and the silicon substrates (see Figure 6.20 (2)) can push generated charge carriers to the bottom or to the top of the substrate. In addition, the electrical scheme shown in Figure 6.20 (1) provides charge carriers the possibility to escape the substrate. Both effects can change the behavior of stray fields affecting the ion. The heating rate was measured at $T = 10\,\mathrm{K}$ using the resolved sidebands method (see chapter 3). The results of the measurements are summarized in Table 6.3.

On day one we measured the heating rate of the ion at $\omega_z = 1\,\mathrm{MHz}$ for three different experimental conditions. With a floating substrate we observed a heating rate of $731(260)\,\mathrm{phonons/s}$ which is significantly higher than the result obtained in previous tests with ungrounded silicon substrate (see section 6.7). When we grounded the substrate, the heating rate decreased to $378(141)\,\mathrm{phonons/s}$. We then applied a $10\,\mathrm{V}$ bias to the substrate and observed a heating rate of $809(112)\,\mathrm{phonons/s}$. For these three measurements we did not manage to cool down the ion to lower than 1 phonon although we did not detect the drift of the micromotion.

On day two we attempted to reproduce the observed results as well as to get data at higher positive bias voltages (+15 V) and at negative bias voltages. The tests with floating, grounded silicon and $+10\,\mathrm{V}$ biased substrate showed heating rates of $\Gamma_\mathrm{h} = 459(49)\,\mathrm{phonons/s}$, $\Gamma_\mathrm{h} = 291(50)\,\mathrm{phonons/s}$ and $\Gamma_\mathrm{h} = 434(61)\,\mathrm{phonons/s}$, respectively. This is a factor of two lower than the results obtained in the previous day. We also managed to cool down the ion to values lower than 0.4 phonons. At $+15\,\mathrm{V}$ bias it was not possible to measure the heating rate because of the issues with ground state cooling at this condition. For negative biases we observed higher heating rates. At $-10\,\mathrm{V}$ and $-15\,\mathrm{V}$ V bias, the heating rates were $\Gamma_\mathrm{h} = 581(75)\,\mathrm{phonons/s}$ and $\Gamma_\mathrm{h} = 1170(187)\,\mathrm{phonons/s}$, respectively. Generally we observed unstable ground state cooling and higher heating rates with negatively biased substrate.

On the third day we attempted to measure heating rates with a positive bias on the substrate. The tests with bias voltages of $+15\,\mathrm{V}$ and $+12\,\mathrm{V}$ showed unstable ground state cooling. Nonetheless $+5\,\mathrm{V}$ bias provided stable conditions for the experiment and a heating rate of $463(86)\,\mathrm{phonons/s}$ was measured.

In conclusion, we observed a day-to-day drift in the heating rate, which was not observed for silicon traps before [44]. In this three-day test, grounding the substrate consistently produced lower heating rates than biasing the substrate with positive or negative voltages.

Table 6.3: Measured heating rate over three days for different biasing voltages. All measurements are performed at $T = 10\,\mathrm{K}$ and the trap with 230 µm electrode-ion separation (fabricated at Infineon). The electrical configuration for applying a bias to the silicon substrate is described in Figure 6.20.

Day	**Heating rate** (phonons/s)	**Substrate bias**
I	731 ± 260	Floating
	378 ± 141	Ground
	809 ± 112	+10 V
II	459 ± 49	Floating
	291 ± 50	Ground
	434 ± 61	+10 V
	Not measured	+15 V
	581 ± 75	-10 V
	1170 ± 187	-15 V
III	Not measured	+15 V
	Not measured	+12 V
	463 ± 86	+5 V

Substrate biasing and charge generation effect

The electrical scheme presented in Figure 6.20 was further used to study the effect of DC electrical biasing on charge carrier generation and on the performance of the RF resonator. The silicon substrate was cooled down to 10 K and 6.62 mW power of 729 nm laser light was used in all experiments listed below. Such an amount of light is the maximum what we can get from our setup.

For all silicon trap chips, we observed that the RF voltage on the electrode is rising only to some certain level while increasing RF input on the resonator, which indicates RF saturation on the chip. This effect limits the performance of the trap chip. Therefore, in the first set of experiments we studied saturation on the trap RF electrode for different light sources. For this we measured the voltage applied at the capacitive divider versus output power of function generator shown in Figure 6.21. The RF amplitude measured at the capacitive divider gives access to the RF amplitude on the trap RF electrode (see section 4). When the input RF power reached $20 - 25$dB we observed saturation of the signal on the

capacitive divider: the amplitude first leveled out, then decreased. We attribute RF voltage saturation on the electrode to local heating of the silicon. The increase in temperature causes an increase of charge carrier density, which in turn increases the loss tangent [81]. The dielectric loss tangent ($\tan\delta_d$) directly relates to the RF dissipation and hence to the quality factor of the resonator, see section 6.1. At around $T = 25\,\mathrm{K}$ $\tan\delta_d$ starts to rapidly rise as well as the quality factor. That causes leveling out and then decrease of the RF voltage (Figure 6.21 (1)).

Then we used the 729 nm laser light overlapped with the ion position. In this case only small part of the light hits the trap surface because of the beam divergence and the strongest reduction of the signal on the capacitive divider has been observed (see Figure 6.21 (2)). During this experiment the substrate was floating. When we grounded the substrate, the RF resonator demonstrates identical behavior for the laser light turned on or off, see in Figure 6.14 (2).

The second set of experiments investigates the influence of the substrate biasing on the RF resonator properties under different light conditions. Figure 6.21 (3) summarizes the data obtained for bias voltages ranging from $+10\,\mathrm{V}$ to $-70\,\mathrm{V}$ in the absence of all light sources. One can clearly see a reduction of the RF amplitude at the capacitive divider at $-70\,\mathrm{V}$ bias. Between $-50\,\mathrm{V}$and $-70\,\mathrm{V}$ we observed a degradation of the resonance properties of the trap chip which is not shown in Figure 6.21. The behavior of the voltage on the RF electrodes was unstable and we did not manage to correctly measure the voltage in this bias voltage range. However, when we biased the substrate with $-70\mathrm{V}$ the resonator response become stable enough to be measured. We observed a significant voltage drop from $\sim 700\,\mathrm{mV}$ to $\sim 500\,\mathrm{mV}$ on the capacitive divider.

We repeated the measurements after a warm up ($T = 310\,\mathrm{K}$) and cool down ($T = 10\,\mathrm{K}$) cycle of the cryostat. Figure 6.21 (4) (blue dots) shows that the quality factor of the RF resonator significantly degraded. We had to attach a voltage amplifier [m] to the function generator to be able to apply higher RF voltages. When we applied more than 26 dBm of power (output of the amplifier) we detected the sudden jump of the voltage. We characterized the resonator with a network analyzer and measured linear gain of 0.133 and reflection coefficient of 64.1 which is comparable with the values obtained before (see Figure 6.16 (1), linear gain is 0.14 and reflection coefficient is 77.9). After this event we achieved much higher RF voltages $> 360\,\mathrm{V}$ on the trap electrode (more than 900 mV on the capacitive divider) without any saturation effect as can be seen in Figure 6.21 (4). This

[m] Mini-Circuits ZHL-5W-1+, 5W

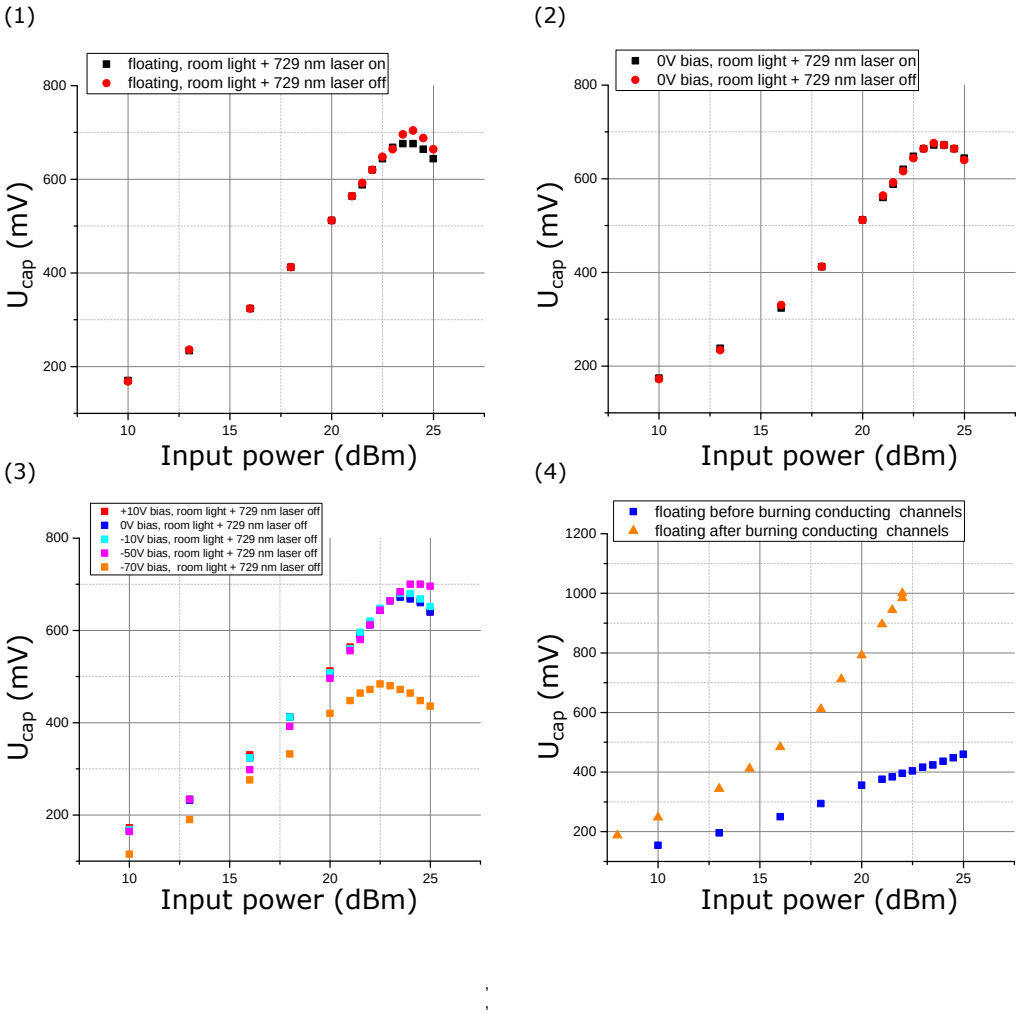


Figure 6.21: Behavior of the RF resonator at $T = 10\,\mathrm{K}$ for different substrate bias voltage and illumination conditions. We measure the voltage applied at the capacitive divider (U_{cap}) versus input power of the resonator (Input power). (1) Silicon substrate is floating. Black dots are data for 729 nm laser light switched on. Red dots are data for 729 nm laser light switched off. (2) Silicon substrate is grounded. Black dots are data for 729 nm laser light switched on. Red dots are data for 729 nm laser light switched off. (3) Silicon substrate is biased ($+10\,\mathrm{V}$, $0\,\mathrm{V}$, $-10\,\mathrm{V}$, $-50\,\mathrm{V}$, $-70\,\mathrm{V}$). 729 nm laser light switched off. (4) The silicon substrate is floating. Blue dots are data obtained before the event of burning conducting channels in the silicon oxide. Orange triangles are data obtained after the event of burning conducting channels in the silicon oxide.

behavior indicates the presence of conducting channels between gold electrode and silicon substrate which leads to the leakage of RF voltage. We associate the origin of this channels with defects in the oxide layer. These defects very probably appear during the fabrication because only the silicon oxidation process underwent significant change compared to the fabrication in FHV (see sections 6.2 and 6.2 for details).

The electrical scheme in Figure 6.20 was further used to measure currents flowing across the silicon substrate. Current across the substrate has a direct correlation with the number of charge carriers in the silicon substrate. During the tests, a trap chip identical to the previous has been used and all DC electrodes on the trap chip were grounded. While the substrate was cooled to 10 K, we measured the RF amplitude on the trap electrode and the current across the DC biased substrate for different light conditions (see Figure 6.22). During the tests the RF voltage of 250 V on the trap electrode was constant. Figure 6.22 (1) and Figure 6.22 (2) show the data obtained when 729 nm laser light was overlapped with the ion position. For $+100$ V of substrate biasing, we measured current of 3125 µA when the laser was switched on and current of 2950 µA when laser was switched off. The higher bias voltages $U_{cap} > \pm 50$ V were able to reduce the Q factor of the resonator down to the 0; see Figure 6.22 (1), (2). The same effect was observed when the 729 nm laser light with 6.5 mW power was pointed towards the trap surface (see Figure 6.22 (3)).

When we applied -250 V of bias voltage to the substrate an electrical breakdown between RF electrode and one of the DC electrodes (grounded) did occur, the current across the substrate went down to zero. During the trap chip installation, no shorts between the RF electrode and DC electrodes have been found. Later when the chip was removed from the cryostat we clearly observed a damaged area with a microscope. Roughly $150 \times 100\,\mu m^2$ of the metal around the gap between electrodes has melted away. Subsequently, it was possible to apply twice higher DC bias voltage without observing the degradation of the RF resonator or current flowing through the substrate (see Figure 6.22 (4)).The resonance frequency of the RF circuit did not change after the electrical breakdown, which indicates that capacitance of the trap chip did not change. We assume that during the electrical breakdown we burned away not only part of the electrode's metalization but also conducting channels in the silicon oxide layer. A similar effect has been observed before with higher RF voltage and no biasing of the substrate; see Figure 6.14 (4).

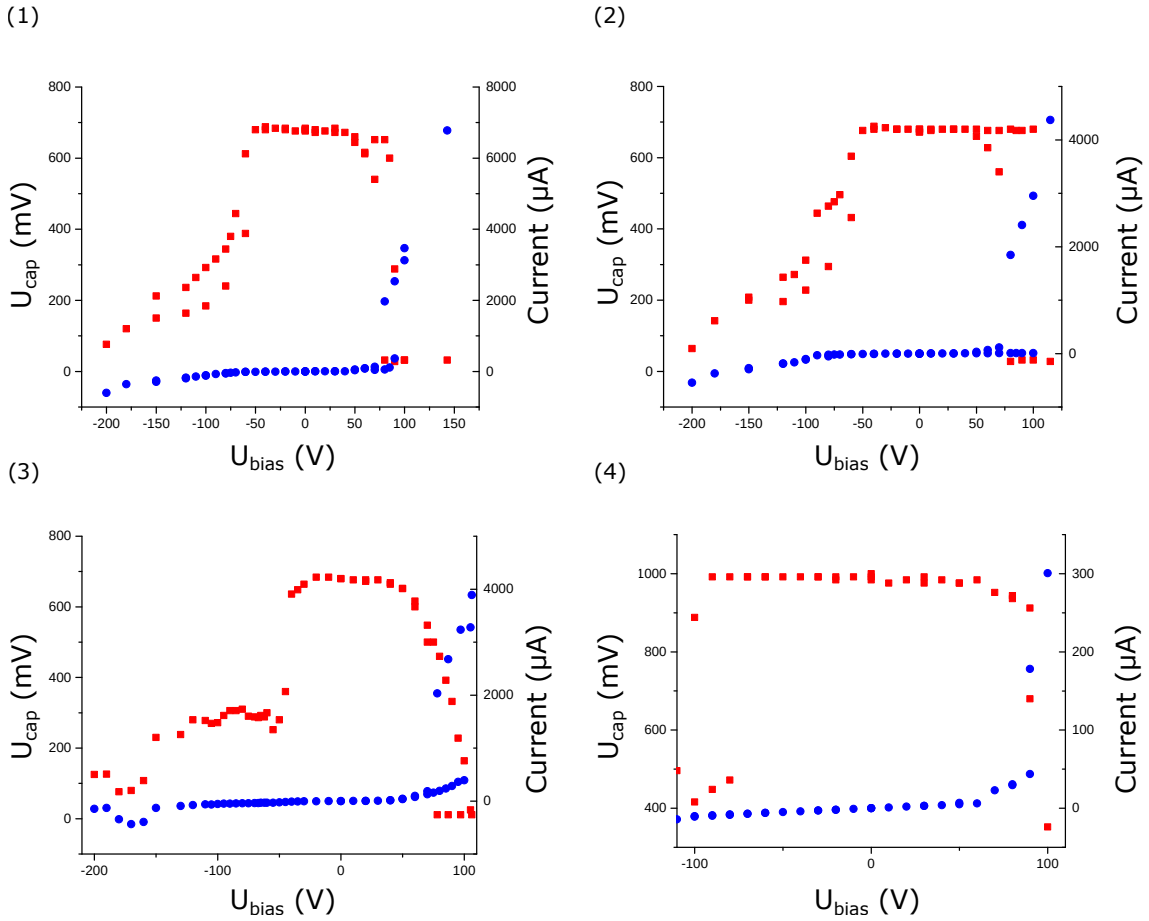


Figure 6.22: Current measured across the substrate as a function of the bias voltage U_{bias} applied to the chip substrate. Blue dots show current across the substrate. Red dots show the signal of capacitive divider. (1) 729 nm laser light was switched on and overlapped with the ion position. (2) 729 nm laser light was switched off and overlapped with the ion position. (3) 729 nm laser light was switched on and pointed towards the trap surface. (4) 729 nm laser light was switched on and pointed towards the trap surface after the electrical breakdown.

CHAPTER 7

Conclusion

Surface ion traps have shown great potential for the realization of large scale quantum computers. In this thesis, a first project focuses on investigating different sources of motional heating in high-temperature superconducting surface ion traps. That project extends an understanding of noise sources, which are limiting quantum algorithms in trapped-ion experiments. In the second project a silicon-based surface ion trap has been studied for the possibility of scaling down the ion-surface separation.

We designed and implemented a surface ion trap with unique topology, as well as a trap chip mount which is capable of changing the trap chip temperature locally, without affecting the cryogenic low-pass filters. We have used a single trapped ion as a probe for bulk and surface properties of materials, achieving the highest sensitivity to electric field noise with a single ion confined in Paul trap reported to date, $S_E = 5.2(11) \times 10^{-16}\,\mathrm{V^2 m^{-2} Hz^{-1}}$ [26]. Our setup integrates an unfiltered on-chip white noise source. We used our ion field probe to non-invasively measure the superconducting transition of YBCO, which was verified with independent on-chip 4-wire resistance measurements. This technique could be used in the future for the characterization of samples that cannot be exposed to a direct resistance measurement, like delicate structures or topologies that cannot be connected. For example, studies of persistent currents in metallic loops, known to be exceptionally sensitive to their

environment [98], might be possible.

Below the transition we measured surface noise with a crossover between two different power-law exponents in the frequency domain. While such a crossover behavior is generally expected [7] and predicted,e.g., by TLF models, to our knowledge it has not been reported in ion trap experiments, which often show power-law frequency dependence of the electric field noise [6]. Our work is the first to show a different frequency dependence. This finding will be of major interest for the study of surface noise in various fields of physics, such as experiments with nitrogen-vacancy centers [48], Casimir effect studies [99], gravitational-wave detectors [100] and trapped-ion systems [6]. The quality and amount of our data in the frequency domain allows us to reliably discriminate between power-law and crossover dependence. The temperature dependence of our data, however, cannot be understood with existing TLF models. Our results, together with other recent studies of noise scaling with ion-electrode distance [56, 35] and chemical composition of surface materials [58, 59, 57], gives new insight into the origin of the anomalous heating rate and surface noise in general. In addition, our work paves the way for the use of high-temperature superconductors for large scale ion-based quantum processors [101], where low-resistance trap electrodes will become important.

Finally, this thesis explored silicon as a challenging, but promising material for surface ion traps [86, 102, 103, 104, 85, 105]. Silicon is a broadly used material in the semiconductor industry, which has developed a variety of techniques enabling the fabrication of highly integrated electronic circuits and processors [106]. However, silicon has high RF losses and cannot be used as-is to make RF ion traps. Until now, there have been two approaches around this issue. One consists in adding an electrode that shields the substrate from the RF [102]; the other one uses highly doped silicon as a conductive electrode material [85, 86]. In this work, we use silicon as a substrate for surface ion traps [9]: below 25 K, the charge carriers in intrinsic silicon freeze out, leaving the substrate as a good insulator with low RF losses. However, during the trap operation, the laser light addressed to the ion can induce charge carriers in the silicon substrate. The band-gap of silicon is 1.17 eV at 10 K [87]. As a result, all laser beams which are used to manipulate the $^{40}Ca^{+}$ ion, have sufficient energy to induce charge carriers in the silicon. The light-induced effect of the charge generation has a profound negative influence on trap performance such as non-compensatable micromotion. This study allows us to examine the potential obstacles caused by such an effect. The trap chips have been characterized by means of micromotion compensation, heating rate measurements and electrical tests of the substrate.

We designed and fabricated silicon-based surface ion traps with electrode-ion separation ranging from 50 µm to 230 µm. The light-induced charge carrier effect was observed for the first time in a $d = 150\,\mu m$ trap chip produced at FHV and UIBK. This effect was verified in a larger trap with $d = 230\,\mu m$ also produced at FHV and UIBK. The production of charge carriers in the bulk of the silicon leads to a drift of the stray fields. It is observed as a drift of the Rabi flopping time on the micromotion sideband which reduces the efficiency of the Doppler cooling. The study of the light-induced charge carrier effect was extended further with a $d = 230\,\mu m$ trap chip produced by Infineon with a modified fabrication process. We introduced additional connections to the silicon substrate in order to study the behavior of a grounded, floating or biased, trap substrate. Experiments with a grounded substrate showed a significant improvement in the stability of micromotion but it was not possible to achieve large Rabi flopping time on the micromotion sideband. Additional biasing of the silicon substrate does not further improve the influence of charge carriers on the micromotion. All of the tested surface ion traps show significantly higher heating rates compared to previous results [9]. Also, we observed a large spread of the values of the heating rate.

Additionally, several electrical tests on trap chips have been performed. We measured that the voltage on the RF electrode is rising only to some certain level while increasing RF input on the resonator, which indicates RF saturation on the chip and limits the performance of the trap chip. We attribute this RF voltage saturation to local RF heating of the silicon substrate. The increase in temperature causes an increase of charge carrier density, which in turn increases the loss tangent [81]. The dielectric loss tangent directly relates to the RF dissipation and hence to the quality factor of the resonator, see section 6.1. That causes leveling out and then decrease of the RF voltage (Figure 6.21 (1)).

The experiments presented in this thesis provide crucial insights into the problems of the heating in surface ion traps which is a primary limitation of current systems. As next step for high-temperature superconducting surface ion traps it will be important to study the different surfaces below the ion. For example, the gold layer can be etched away so that the ion will be directly exposed to the ceramic material (YBCO); see section 5.2. Concerning silicon-based surface ion traps, the fact that we were not able to eliminate the generation of charge carriers creates a significant obstacle for further projects based on this fabrication technique [9].

CHAPTER 8

Appendix

8.1 SNU trap

The following project has been performed in collaboration with the Nano/Micro Systems and Controls laboratory at Seoul National University (SNU). They provide us with the Thin Track I trap chip which has the following important aspects:

1. Dielectric pillars are coated with metal in order to avoid direct exposure of the ion to the dielectric surfaces

2. Additional metal coating of the trapping region in order to improve the trap performance. 10 nm of titanium were used as an adhesion layer for 100 nm of gold

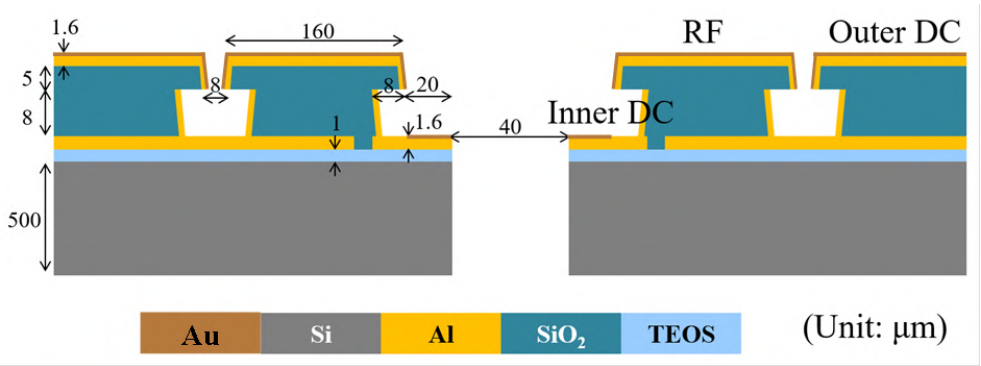
3. The trap chip size has been minimized to achieve optimal access to the trapping zone with the laser beams from the side of the chip

4. The trapping region is 616 µm long with full-length loading slot under it;

5. Eight segmented DC electrodes for ion manipulation

6. A pair of inner DC rails fabricated on the ground metal layer for tilting a principal axis of the potential

(1)



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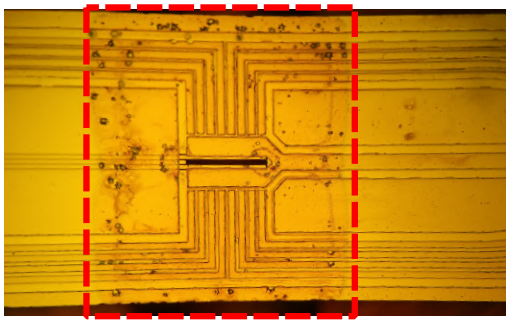

(3)

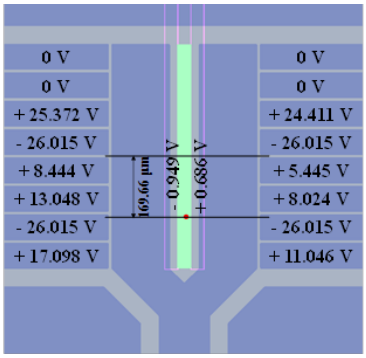

Figure 8.1: (1) The scheme of vertical cut of the Thin Track I ion trap. Figure courtesy of Dan Cho. (2) The microscope pictures of the central ion trapping region with pronounced gold plague pattern. (3) The voltage scheme which was used to trap an ion, provided by SNU.

In Figure 8.1 (1) the scheme of a vertical cut of the trap chip is presented with characteristic dimensions. After detailed inspection we found that the central region of the chip which is coated with gold, has patterned structures see Figure 8.1 (2). We believe that it is gold plague, a compound of gold and aluminum which formed between the layers.

Such a design allows us to trap an ion $\sim 65\,\mu m$ above the surface. Our goal was to reach an axial frequency of 1 MHz and a radial frequency of 6 MHz with reasonable trap depth and stability parameters. We reached the axial frequency with a voltage scheme presented

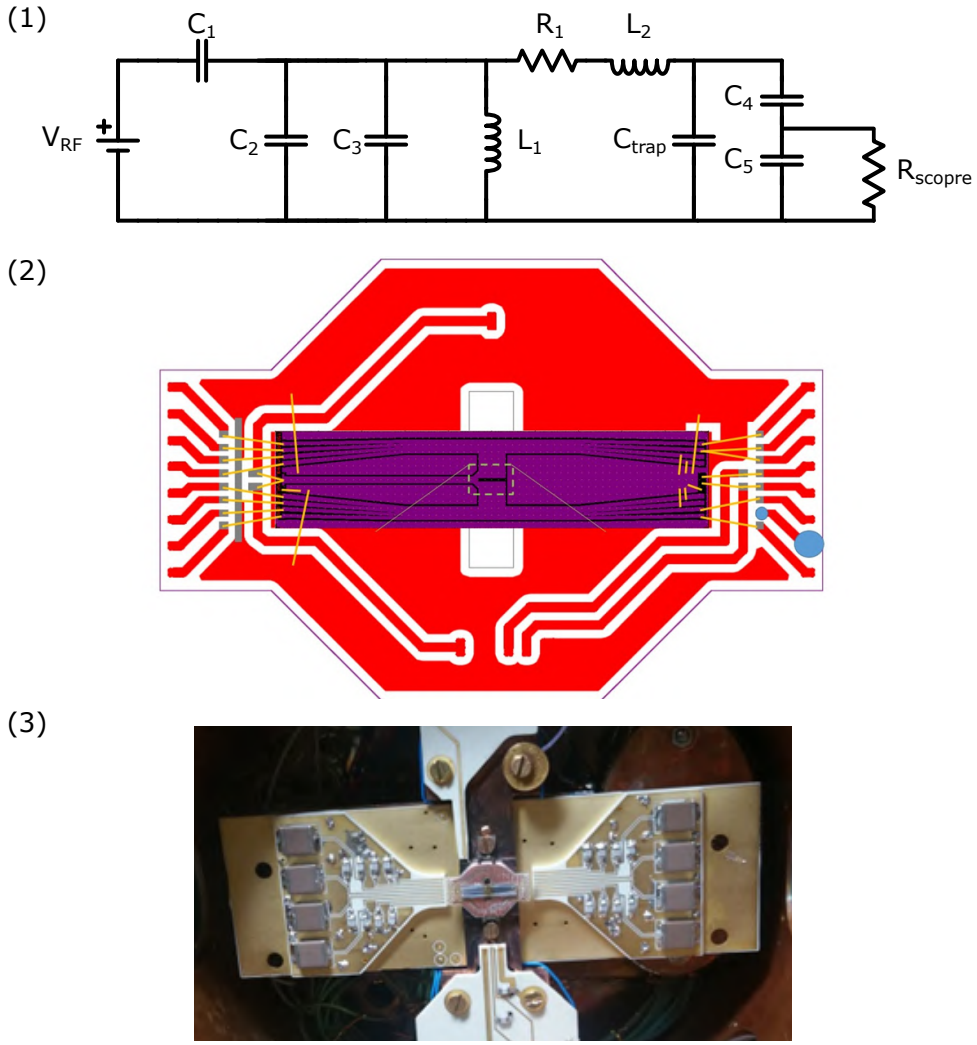

Figure 8.2: (1) The RF circuit consist of a matching network (two adjustable capacitors $C_1 = 12 - 100\,\text{pF}$, $C_2 = 12 - 100\,\text{pF}$ and one fixed capacitor $C_3 = 47\,\text{pF}$), RF resonator (choke inductance $L_1 = 1\,\mu\text{H}$, resistance $R_1 = 4.4\,\Omega$ and inductance $L_2 = 0.86\,\mu\text{H}$ of the resonator coil as well as trap capacitance $C_{trap} = 7\,\text{pF}$) and capacitive divider ($C_{trap} = 2.5\,\text{pF}$, $C_5 = 1000\,\text{pF}$). (2) Adapter PCB for SNU Thin Track I chip. On the picture below you can find scheme of adapter PCB (red) with bonded trap (purple) and bonding wires (yellow). (3) The picture of the SNU Thin Track I chip with adapter PCB and RF circuit inserted inside of the cryostat.

in Figure 8.1 (3). The q-parameter of 0.3 and trap depth of 160 meV were achieved by using 58 MHz of RF drive frequency with 123 V amplitude on the trap. We designed a

new RF circuit (Figure 8.2 (1)) and adapter PCB board (Figure 8.2 (2)) to fullfill electrical criteria and to interface the Thin Track I trap layout to cryo setup.

The RF resonator was built using a $L_2 = 0.86\,\mu H$ toroidal resonator coil (Figure 8.2 (1)). The resonance was at 57.8 MHz. The resonator was impedance matched using two adjustable capacitors (C_1 and C_2) and a test chip. When the PCB was inserted into the cryostat the circuit matching was completely gone, no resonance peak could be observed at the target frequency. We used an RF amplifier to get the required RF voltage using the capacitive divider signal as reference for the actual voltage on the trap. We assumed the nominal capacitive divider ratio of 1/400. Additionally to ensure solid thermal and mechanical connection in cryostat several gluing tests were performed. Dummy chips were used for that purpose. We tried Epotec epoxy H20E-PFC, Epotec epoxy H24 and superglue. H24 passed liquid nitrogen tests and was used in the following experiments. The completely assembled trap setup which is mounted inside of the cryostat is presented on the Figure 8.2 (3).

After cooling down the cryostat we used the following parameters for ion trapping: 53.1 MHz of RF voltage with amplitude from 90 V to 120 V. According to our simulations this corresponds to around 5 MHz to 7 MHz radial frequency.We used the voltage calculated from the Seoul University for a trapping position 170 µm away from the trap center towards the closed end of the RF fork Figure 8.1 (3). We used the cage system [80] for highly elliptical 397 nm and 866 nm Doppler cooling beams from one view port. The 377 nm and 422 nm PI beams were applied from the opposite side of the chamber.

Under these conditions, trapping was unreliable. Cooled storage times were only seconds up to half a minute. The loading rate was fluctuating strongly from 1 per every few seconds to 1 per 10 minutes or more. This seemed not to depend on external parameters: we varied micromotion compensation in all direction up to a few volts, varied the RF confinement and DC confinement, power and frequency of Doppler lasers. In conclusion, we assume that the trap surface was spoiled by gold plague. This played an important role in the trapping and the stability of the ion. The trap fabrication has to be improved, namely introduce diffusion barrier like platinum in between aluminum and gold.

8.2 Electric field noise spectra of the technical noise with the different origin below T_c

Our main goal in the regime below T_c was to observe the heating rate spectra dominated by surface noise; see section 5. One of the obstacles was to mitigate the technical noise sources which can overwhelm the low level noise signal from the surface. The origin of technical noise sources can vary from one experimental setup to another hence detection of these sources can be a challenging task. In our case we chose to measure and analyze heating rate versus axial frequency scans to identify the amplitude and the spectral properties of the noise sources.

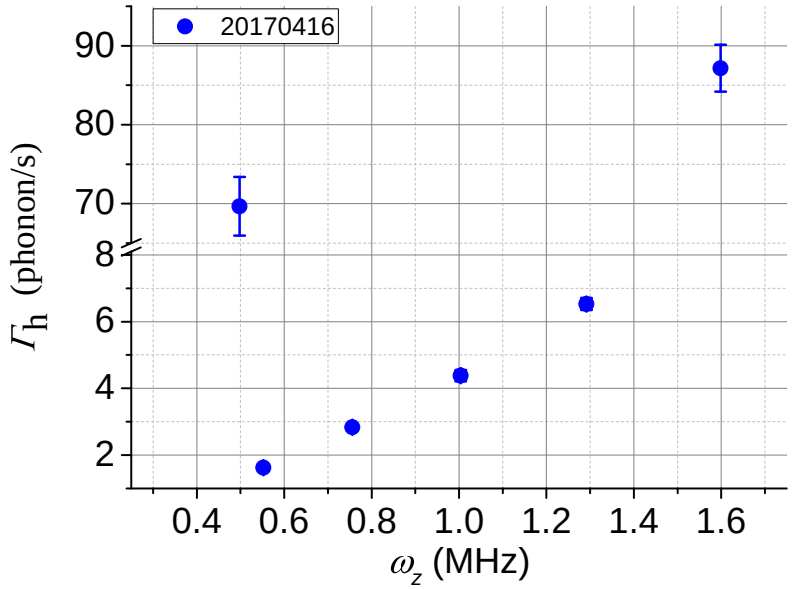

Figure 8.3: The heating rate spectrum at the temperature 11.4 K dominated by the noise source which has its origin in the temperature of the controlling circuit.

Our first measured heating rate spectrum below the superconducting transition, see more details of the experiment in the section 5, is presented in Figure 8.3. The heating rate is linearly rising in the $0.55-1.3$ MHz frequency range from $\Gamma_h = 1.62(7)$ phonons/s to $\Gamma_h = 6.53(18)$ phonons/s. Note that at 0.5 MHz the heating rate is $\Gamma_h = 69.7(40)$ phonons/s and at 1.6 MHz the heating rate is $\Gamma_h = 87.2(30)$ phonons/s which can indicate a presence of peaks in the spectrum. Such a spectrum clearly indicates technical noise influence. We found a significant improvement of the spectrum, see Figure 8.4, on the level of the noise

as well as on the spectral properties if the temperature controlling unit (see section 4.1), is disconnected from the cryostat and the corresponding wires are shorted to ground. For this project an additional temperature sensor was glued in close proximity to the trap hence DC and RF bonding wires have signal pick-up from the temperature controlling unit; see Figure 5.5 (1).

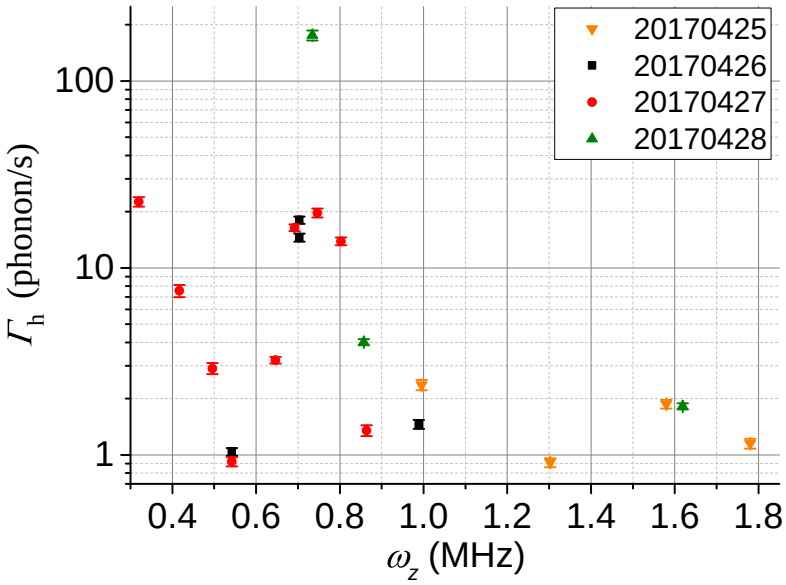

Figure 8.4: The heating rate spectrum at the temperature 11.4 K dominated by the noise source which was picked up on the room temperature pi filter.

In Figure 8.4 we observe a general decrease of the noise amplitude in the $0.55-1.6$ MHz frequency range however two pronounced peaks at 0.7 MHz and 1.6 MHz have been detected. Frequencies of these peaks are reproducible; note different measurement days on right corner of the Figure 8.4. We also observed that the noise level of the peak at 0.7 MHz was fluctuating from $\Gamma_h = 16.4(7)$ phonons/s to $\Gamma_h = 176(11)$ phonons/s. Such behavior is caused by external room temperature DC pi filters; see Figure 8.5. The pi filter is built on a homemade PCB board using two capacitors $C_1 = 0.1\,\mu$F, $C_2 = 0.68\,\mu$F and one inductance $L_1 = 470\,\mu$H with a cut-off frequency of 17 kHz (Figure 8.5). The PCB board of these filters was damaged and the filter setup was acting like an antenna for the noise sources in the laboratory. After the pi filters were removed, the heating rate level was drastically suppressed and no peaks in the spectrum were observe (see Figure 5.13).

In conclusion, to our knowledge [6], all above listed manipulations with the experimental setup allowed us to observe the heating rate as low as $\Gamma_h = 0.051(10)$ phonons/s at

$T = 12\,\mathrm{K}$, $\omega_z = 2\pi \times 1.51\,\mathrm{MHz}$ and the crossover regime in the frequency spectra of the heating rate for different temperatures below T_c; see section 5.7.

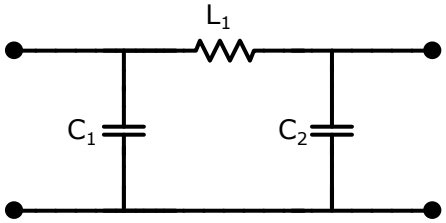

Figure 8.5: The room temperature pi filter consist of $C_1 = 0.1\,\mu\mathrm{F}$, $C_2 = 0.68\,\mu\mathrm{F}$ and $L_1 = 470\,\mu\mathrm{H}$

8.3 Deep reactive ion etching (DRIE)

Deep reactive ion etching (DRIE) is one of the crucial processes for development of different micro-electro-mechanical systems (MEMS) [107]. In addition to that DRIE has found implementation in surface ion traps [9, 85]. This process serves to produce deep trenches in silicon substrate by means of several cycles of alternating polymer deposition and silicon etching. The required aspect ratio of trench can be achieved by adjusting the parameters of the individual scallops (formed by one cycle of deposition and etching).

The c-C_4F_8 is used to create a protective layer on the sidewalls of the silicon trench from the etching step. The SF_6 selectively etches the bottom of the trench. In Figure 8.6 we present a detailed process of DRIE. The first step starts with creating the masking layer which can be realized it two ways: a soft mask produced from the photoresist and a hard mask made of dielectric layer, for instance SiO_2. The second step forms the layer of polymer $(CF)_x$ which is polytetrafluoroethylene (PTFE). In order to form PTFE a plasma breaks the strained cyclic hydrocarbon c-C_4F_8 into the fragments:

$$c - C_4F_8 + e^- \longrightarrow 2C_2F_4 \longrightarrow C, F, CF, CF_2, CF_3\,(\text{gas phase})\,. \tag{8.1}$$

Then on the exposed silicon surface individual fragments of C_2F_4 and CF_2 react between each other and build a polymer layer [108], [109]:

$$C_2F_4, CF_2 \longrightarrow (CF)_x\,(\text{polymerization on the surface})\,. \tag{8.2}$$

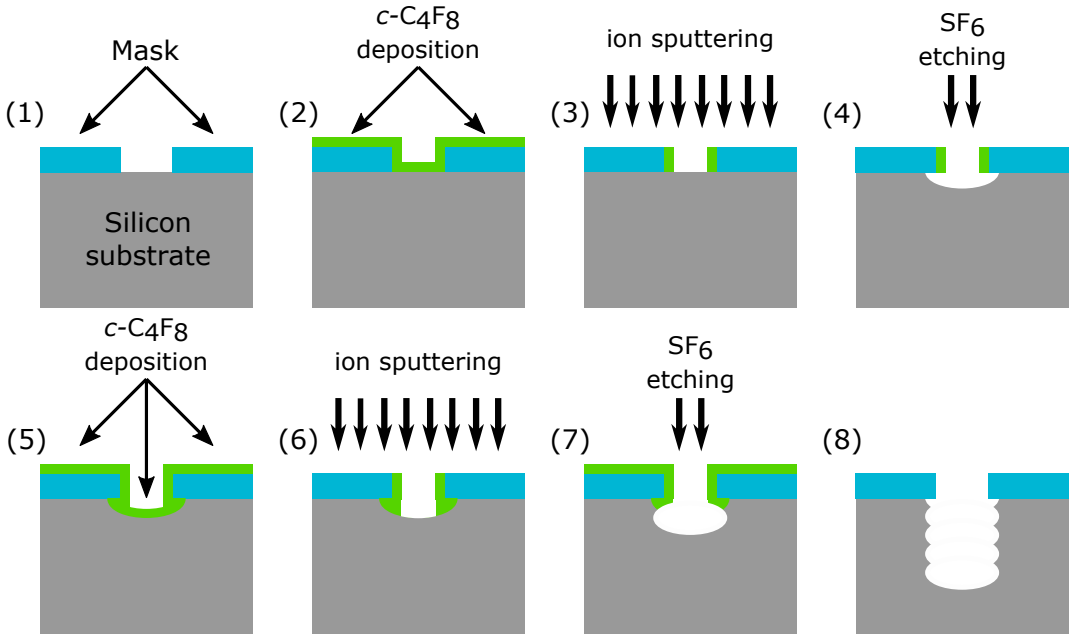

Figure 8.6: Steps of alternating deposition and etching for DRIE process.

This process is called plasma polymerization. The next step of ion sputtering removes a horizontal layers of $(CF)_x$ and leave horizontal parts of sidewall protection (Figure 8.6 (3)). The fourth step is SF_6 etching. The chemical reactions occurred in the gas phase are [110]:

$$SF_6 + e^- \longrightarrow SF_{3,4} + (3,4)F + e^- . \tag{8.3}$$

On the surface of the substrate, the silicon is removed with the following reaction:

$$Si_{solid} + 4F \longrightarrow (SiF_4)_{gas} . \tag{8.4}$$

In Figure 8.6 (5)-(7) we show steps, explained in the details above. These steps are repeated to form scallop-like structure Figure 8.6 (8) with desired aspect ratio.

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