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infineon

Development of novel micro-fabricated ion traps

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Abstract

Quantum computers and quantum simulators operate on qubit registers to outperform classical computers. Trapped ions are a promising platform for such devices because the degree of precision achieved in the quantum manipulation of trapped ions allows for quantum error correction, a key requirement for large-scale quantum devices. The development of scalable trap architectures thus moves into the focus of research groups. With micro-fabricated surface traps, a solution seems to be in sight. The control needed to reasonably use thousand of ions in experiments calls for complex trap designs with more individual electrodes and integrated electronics. Such traps can only be reliably and reproducibly fabricated in cooperation with experts from semiconductor industry.

This work presents the results of the first ion traps developed in cooperation between the University of Innsbruck and Infineon Technologies. One trap type could be manufactured and tested and another designed and simulated. Furthermore, the success of this work and the constructive cooperation of the participants paved the way for the follow-up project PIEDMONS [1] .

Kurzfassung

Quantencomputer und Quantensimulatoren arbeiten mit Qubit-Registern um klassische Computer zu übertreffen. Gefangene Ionen sind dafür eine vielversprechende Plattform, da der bei den Quantenmanipulation erreichte Genauigkeitsgrad, Quantenfehlerkorrektur ermöglicht, eine Schlüsselanforderung für Quantenbauelemente mit vielen Qubits. Die Entwicklung skalierbarer Fallenarchitekturen rückt somit in den Fokus der Forschungsgruppen. Mit Mikro-fabrizierten Oberflächenfallen scheint eine Lösung in Sicht. Die benötigte Kontrolle, um tausende Ionen vernünftig in Experimenten nutzen zu können, verlangt nach komplexen Fallendesigns mit mehr einzelnen Elektroden und integrierter Elektronik. Solche Fallen können nur in Zusammenarbeit mit Experten aus der Halbleiterindustrie zuverlässig und reproduzierbar hergestellt werden.

Diese Arbeit präsentiert die Ergebnisse der ersten Ionenfallen, die innerhalb einer Kooperation zwischen der Universität Innsbruck und Infineon Technologies entstanden sind. Dabei konnte ein Fallentyp gefertigt und getestet werden und ein weiterer designed und simuliert. Des Weiteren wurde durch den Erfolg dieser Arbeit und die konstruktive Zusammenarbeit der Beteiligten der Weg für das Nachfolgeprojekte PIEDMONS geebnet.

[1] Portable Ion Entangling Devices for Mobile-Oriented Next-generation Semiconductor-technologies

Contents

Chapter 1

Introduction

Integrated circuits (ICs) and computer chips form the basis of a wide range of everyday applications like TVs, laptops, smart phones and smart watches. Furthermore, ICs enable the development of new applications such as vehicles for autonomous driving. These applications are only feasible, because the computing power of the ICs was improved again and again, which was possible by a steady down scaling of the transistor's size. During the last five decades, the number of transistors per area in ICs doubled approximately every 24 months, an empirical scaling law know as Moore's law [1].
As Moore's law is expected to end [2], the field of quantum computing has emerged to provide an alternative to classical computing. Already in 1982 Richard P. Feynman proposed that quantum mechanical problems could best be solved by computers using the laws of quantum mechanics [3]. For quantum computation there exist specific quantum algorithms, which can solve certain computational problems much faster than classical ones, e.g. Shor's algorithm for prime factorization [4] or Grover's algorithm for browsing unsorted databases [5].
The fundamental difference between classical and quantum computation is the way how information is processed. While classical computers use bits, which can either be 0 or 1, a quantum computer uses quantum bits, in short "qubits". These qubits are quantum mechanical two-level systems, with states referred to as $|0\rangle$ and $|1\rangle$, respectively. Unlike classical bits, qubits cannot only be either $|0\rangle$ or $|1\rangle$, but also superpositions of these two states are possible.
Various quantum mechanical systems seem to be suitable for this purpose [6–11]. In 2000, David DiVincenzo suggested a list of criteria, which need to be fulfilled by a quantum mechanical system, in order for it to be used for quantum computing [12]. According to this list, the requirements are as follows:

(1) A scalable physical system with well characterized qubits

(2) The ability to initialize the state of the qubits

(3) Long relevant decoherence times, much longer than the gate operation time

(4) A universal set of quantum gates

(5) A qubit-specifc measurement capability

One of the most promising systems for building a quantum computer is the use of trapped ions as qubits [13, 14]. Paul traps can confine chains of ions by combining static and dynamic electric fields [15]. In addition, lasers allow me to manipulate the quantum states of the ions. Many successful experiments concerning quantum simulation [16–18] and quantum computing [19,20] have already demonstrated the great potential of this quantum system.

However, research groups are currently facing the challenge of scaling to larger qubit numbers. Only then will it be possible to outperform classical supercomputers. In order to reasonably work with hundreds or thousands of ions, it is necessary to have extremely precise experimental control over the ions. This includes the ability to split long strings, move individual strings, and reunite the pieces as desired [21]. Micro-fabricated traps that provide such a high degree of experimental control require a variety of electrodes to control the ions accordingly.

One step towards fabrication of such traps is to cooperate with industry partners such as Infineon Technologies. The industrialization of the trap production has several advantages:

- **High reproducibility of fabrication:** Compared to the conditions in a university cleanroom, industrial production facilities are maintained more frequently to keep processes within tight specifications. Constant monitoring of the process parameters ensures reliable reproducibility.
- **More fabrication processes available:** The variety of products manufactured at Infineon Technologies requires a wide range of processes. Among them are very specialized processes that are unlikely to be found in university clean rooms, such as the structuring of several metal layers with vias, high resolution lithography, the application of thick metal layers or wafer bonding. This large selection can be used and adapted to produce new ion traps.
- **Flexible implementation of process changes:** The individual production processes are collected in a workflow. Changes, such as a variation of the thickness of a deposited layer or even adding processes such as additional cleaning steps or defect monitoring can be implemented in a relatively flexible way.
- **Extended capabilities of failure analysis:** Failure analysis tools at Infineon Technologies in Villach offer many possibilities to monitor the production process of the traps and to test the finished products. For example, defects or air pockets in oxide layers could lead to failures during the experiment and can be ruled out in advance.

The aim of this work was to take the first step in a cooperation between the University of Innsbruck and Infineon Technologies. It was about getting introduced into the organization behind an industrial fabrication and highlight the benefits resulting from the cooperation for both sides. This master's thesis is structured as follows: the theoretical background for ion trapping with Paul traps and the description of quantum bits are introduced in Chapter 2. Chapter 3 deals with the scalability of on-chip ion traps and introduces the problem of heating. In Chapter 4, the two trap designs are presented and described by

means of simulations. Chapter 5 gives a general description of the work in an industrial clean room and of the fabrication of the traps. The individual processes are introduced and explained. Furthermore, we describe the failure analysis used to validate the traps before they are installed in the ion trapping setup. The experimental setup, which includes details about the vacuum chamber and the optical setup is described in Chapter 6. Chapter 7 presents the experimental results from the characterization of the traps. Finally, Chapter 8 summarizes this work.

Chapter 2

Principles of ion trapping

The experiments described in this thesis operate with laser-cooled $^{40}Ca^{+}$ ions. The ions are confined in linear Paul traps. The physical background of this kind of trapping is discussed in the following chapter. Additionally, the energy levels of $^{40}Ca^{+}$ and the used optical transitions are introduced.

2.1 Paul traps

Ion traps that use a combination of static (DC) and time-varying (AC) electric fields to trap charged particles are called Paul traps, after their inventor Wolfgang Paul [15]. The AC field is generated by applying a radio-frequency (RF) voltage to electrodes of the trap, hence their other designation "RF ion traps".

2.1.1 Physical principle

The goal of using a Paul trap is to confine a charged particle in a three dimensional harmonic potential. This potential can be written as

$$U(x,y,z) = \frac{1}{2}(k_x x^2 + k_y y^2 + k_z z^2), \tag{2.1}$$

where k_i is defined as $k_i = \partial_i^2 U$ with $i \in \{x,y,z\}$. Trap frequencies $\omega_{\mathrm{T}i}$ of a particle with mass m can then be calculated by

$$\omega_{\mathrm{T}i} = \sqrt{\frac{k_i}{m}}. \tag{2.2}$$

For a particle with electric charge Q, the electric trapping potential can be written as

$$\phi(x,y,z) = \frac{U(x,y,z)}{Q} = \frac{1}{2Q}(k_x x^2 + k_y y^2 + k_z z^2). \tag{2.3}$$

As every electric potential in free space needs to fulfill Laplace's equation,

$$\Delta\phi(x,y,z) = \frac{1}{Q}(k_x + k_y + k_z) = 0, \tag{2.4}$$

at least one curvature k_i must be negative. For a positive charged particle the negative curvature causes an anti-trapping potential along the corresponding direction. This fact leads directly to Earnshaw's theorem, which states that static magnetic or electric fields cannot create a stable stationary equlibrium in three dimensions for a charged particle [22]. In linear Paul traps a three-dimensional trapping potential can not be created by only static electric fields. However, an alternating quadrupole potential can achieve stable trapping along two directions.

Figure 2.1.a shows a plot of such a quadrupole potential, with trapping along x direction and anti-trapping along y direction. If one varies the voltage with the right frequency, trapping in both directions can be achieved. The effective potential seen by the ion is called pseudopotential with its minimum at the same position as the saddle point of the quadrupole potential itself. The ion is trapped at the point where the RF field vanishes. Otherwise the ion is held constantly moving by the RF field. Such movement is called micromotion and needs to be suppressed by keeping the ion in place.

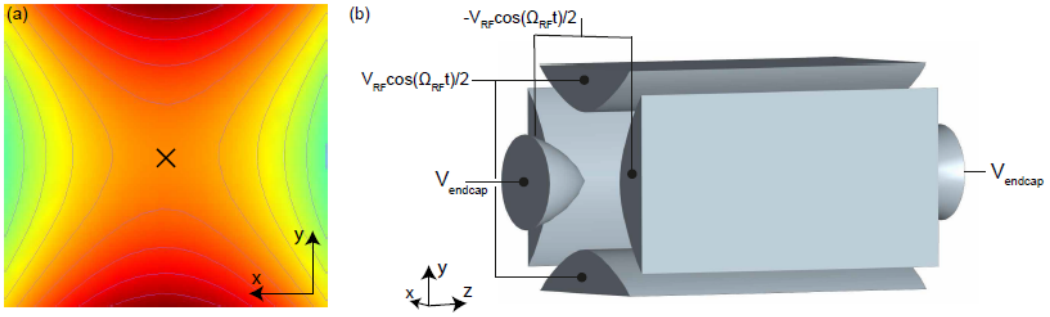


Figure 2.1: (a) Quadrupole potential created by the electrodes of a three-dimensional Paul trap with trapping along x direction and anti-trapping along y direction. The saddle point is marked with the black cross. Time-varying the voltages at frequency Ω_{RF} creates a pseudopotential which enables trapping along both directions. **(b)** Schematic of a linear three-dimensional Paul trap. By applying an alternating voltage with amplitude $\pm V_{\mathrm{RF}}/2$ at the hyperbolic electrodes, trapping along x and y direction is obtained. An additional DC voltage (V_{endcap}) at the endcap electrodes generates axial confinement along z. Figure taken from [23].

A schematic of a linear Paul trap is shown in figure 2.1.b. An RF voltage, applied to the hyperbolicly shaped electrodes, with amplitude $\pm V_{\mathrm{RF}}/2$ and frequency Ω_{RF}, generates an alternating quadrupole potential. The voltages of opposite electrodes have a 180° phase shift against each other. The electric potential of this situation can be written as

$$\phi(x,y,z,t) = \frac{V_{\mathrm{RF}}}{2R_0^2}(x^2 - y^2)\cos(\Omega_{\mathrm{RF}}t), \tag{2.5}$$

where $2R_0$ is the smallest distance between two opposite electrodes. The frequency of the quadrupole potential, Ω_{RF}, is often called the trap-drive frequency. The movement of a

charged particle within this potential can be described by a set of differential equations, which is a special form of Mathieu's differential equations [15]:

$$\ddot{x} - \frac{q\Omega_{\mathrm{RF}}^2}{2}\cos(\Omega_{\mathrm{RF}}t)x = 0 \tag{2.6}$$

$$\ddot{y} + \frac{q\Omega_{\mathrm{RF}}^2}{2}\cos(\Omega_{\mathrm{RF}}t)y = 0 \tag{2.7}$$

$$\ddot{z} = 0. \tag{2.8}$$

The corresponding stability parameter q is defined as

$$q = \frac{2QV_{\mathrm{RF}}}{mR_0^2\Omega_{\mathrm{RF}}^2}. \tag{2.9}$$

With only the alternating quadrupole potential (pseudopotential), and no additional DC fields along the z axis, one finds stable trapping along x and y direction for $q \leq 0.91$ [24]. This regime of the stability parameter is called pseudopotential approximation. A charged particle within this trapping potential is not standing still [25] as is illustrated in figure 2.2. The actual movement can be decomposed into two individual oscillations.

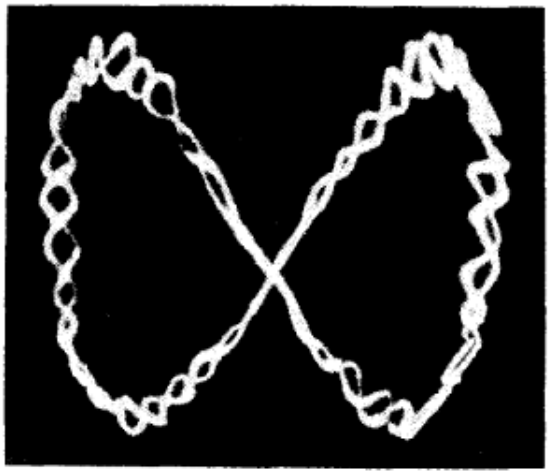


Figure 2.2: Microphotograph of a single charged particle of aluminum dust confined by a two-dimensional quadrupole potential. The planar 2:1 Lissajous trajectory is superimposed by micromotion. Figure taken from [25].

The first one is an oscillation at the trap-drive frequency, Ω_{RF}, itself. This oscillation is called micromotion and is typically unwanted. It can be reduced by trapping the ion at the minimum of the pseudopotential, as the electric RF field vanishes at this point. Residual stray fields and accumulated charges at the electrode surfaces can push the ion away from this position and lead to an increase of micromotion. During the experiment one typically uses DC fields to compensate stray fields and minimize the micromotion. If the compensation is not done properly, this causes a reduction of the laser cooling efficiency [26].

The second oscillation is called secular motion and its frequency is

$$\omega_{\mathrm{Tx,y}} = \frac{q\Omega_{\mathrm{RF}}}{2\sqrt{2}}. \tag{2.10}$$

Therefore, the frequency of the secular motion is smaller, but its amplitude is typically bigger than the corresponding values for micromotion. This movement can be seen as the movement of a particle trapped in the pseudopotential, $\phi_{\mathrm{Pseudo}}(x, y, z)$, which is given by

$$\phi_{\mathrm{Pseudo}}(x, y, z) = \frac{Q^2}{4m\Omega_{\mathrm{RF}}^2} |\nabla \phi_{\mathrm{max}}(x, y, z)|^2, \tag{2.11}$$

where $\phi_{\mathrm{max}}(x, y, z)$ refers to the maximum value of $\phi(x, y, z, t)$, that occurs for $\cos(\Omega_{\mathrm{RF}} t) = 1$. Together with equation 2.5, the pseudopotential in a Paul trap can be written as

$$\phi_{\mathrm{Pseudo}}(x, y, z) = \frac{Q^2 V_{\mathrm{RF}}^2}{4m\Omega_{\mathrm{RF}}^2 R_0^4}(x^2 + y^2). \tag{2.12}$$

In this form it is easy to see that the pseudopotential is a harmonic potential that provides trapping along x and y direction (radial confinement). A typical value for the smallest distance between the trapped ions and the electrodes for a traditional linear Paul trap like those used in Innsbruck is $R_0 = 0.5 - 0.6\,\mathrm{mm}$ [27]. The used RF voltage has an amplitude of $V_{\mathrm{RF}} \approx 2$ kV and the corresponding trap drive frequency is $\Omega_{\mathrm{RF}} = 2\pi \cdot 16\,\mathrm{MHz}$ which results in trap frequencies $\omega_{\mathrm{Tz}} = 2\pi \cdot 700\,\mathrm{kHz}$ and $\omega_{\mathrm{Tx,y}} = 2\pi \cdot 1.8\,\mathrm{MHz}$ [27]. Usually the RF voltage is applied to only one pair of electrodes instead of using $\pm V_{\mathrm{RF}}/2$ for both pairs of electrodes. This simplifies the experiment, because there is no need to keep the voltages phase locked.
As said before, the pseudopotential provides trapping in radial direction. For additional axial confinement (along z direction) one needs to apply a DC voltage to the end cap electrodes (see figure 2.1.b). Typically the axial trap frequency is chosen to be smaller than the radial ones, $\omega_{\mathrm{Tz}} < \omega_{\mathrm{Tx,y}}$, so the DC voltage is adjusted accordingly.

2.2 Electronic energy levels of $^{40}Ca^+$ ions

Various species of atomic ions are suitable for quantum computing experiments [28]. However, there are many requirements that need to be fulfilled. The atoms should be stable and provide a simple energy-level structure after being ionized. Typically, the level structure of singly ionized alkaline earth atoms (Be^+, Mg^+, Ca^+, Sr^+) is very similar to the energy level scheme of neutral alkali atoms, in particular to atomic hydrogen. This includes a metastable state that can be used to encode a qubit (not in Be^+ and Mg^+) . Additionally, the other necessary atomic transitions need to be in or at least close to the optical range with a laser available to drive them.
The ion traps discussed in this thesis are designed to trap laser cooled $^{40}Ca^+$ ions. The lowest energy levels of a singly ionized Ca atom and the corresponding Zeeman sublevels are shown in figure 2.3.

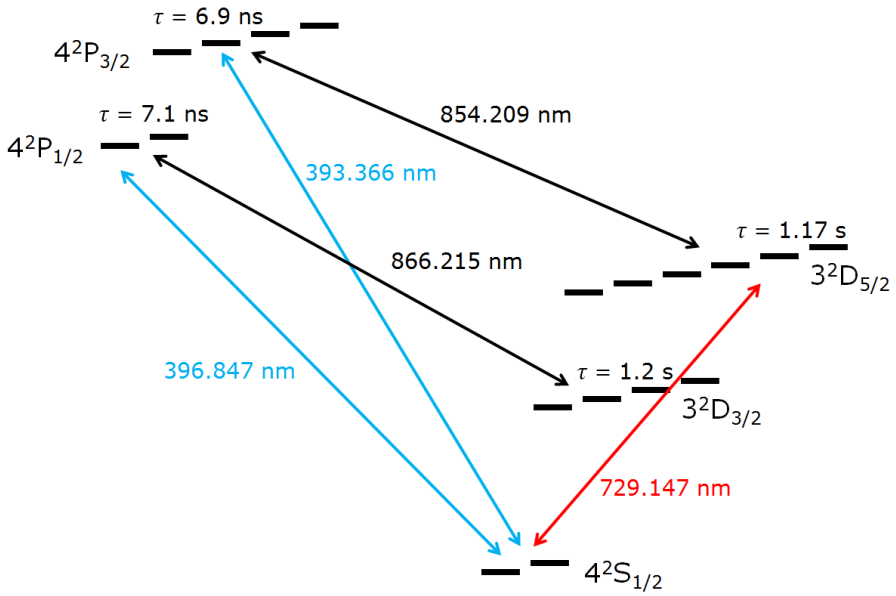


Figure 2.3: The lowest energy levels of a singly ionized ^{40}Ca atom and the corresponding Zeeman sublevels. The wavelengths of the different transitions and the natural life times of the excited states, τ, are given [29–31]. The 729 nm transition is a quadrupole transition that is used for encoding the qubit, as well as for ground-state cooling and heating rate measurements. The dipole transition at 397 nm is used to detect the qubit state and for Doppler cooling. For repumping from the meta-stable D-states to the S-states, two lasers at 866 nm and 854 nm are used.

For the first discussion of the different transitions of the $^{40}Ca^{+}$ ion, the Zeeman sublevels are neglected. The electric ground state is the $4^2S_{1/2}$ state. The D-levels ($3^2D_{3/2}$, $3^2D_{5/2}$) are the next higher levels in the scheme. They are energetically separated due to spin-orbit coupling. As the transition from S to D is a quadrupole transition and electric-dipole forbidden, the D-states have a relatively long life time of around 1 s. Laser light with 729 nm wavelength is used to drive the transition from $S_{1/2}$ to $D_{5/2}$. These two states are used to encode the qubit and in this context they are often written as $|S\rangle$ and $|D\rangle$, respectively.

Two P-levels, $4^2P_{1/2}$ and $4^2P_{3/2}$, with allowed dipole transitions to the 4S- and 3D-states, are also important to run the experiments. Both have a short life time of roughly 7 ns. In particular, the $4^2S_{1/2}$ - $4^2P_{1/2}$ transition at 397 nm, is used for Doppler cooling and state detection. As the probability for a decay from $4^2P_{1/2}$ to $3^2D_{3/2}$ is around 7.5 %, there is an additional laser at 866 nm for repumping, that reduces the occupation of the D-state during the cooling and detection processes. A second repumping laser at 854 nm is used to initialize the state of the qubit. This is done by pumping the population from $3^2D_{5/2}$ to $4^2P_{3/2}$ from where it decays quickly to the ground state.

As mentioned before, this was a description of the situation without considering the Zeeman sublevels. These levels are energetically degenerate as long as there is no external magnetic field present. During the reported experiments, a magnetic field of several gauss is applied. The magnetic splitting of the $3^2D_{5/2}$ sublevels is 1.68 MHz/G, whereas the splitting of the $4^2S_{1/2}$ sublevels is about 2.80 MHz/G. Figure 2.4 shows the additional transitions from $4^2S_{1/2}$ to $3^2D_{5/2}$ after lifting the degeneracy.

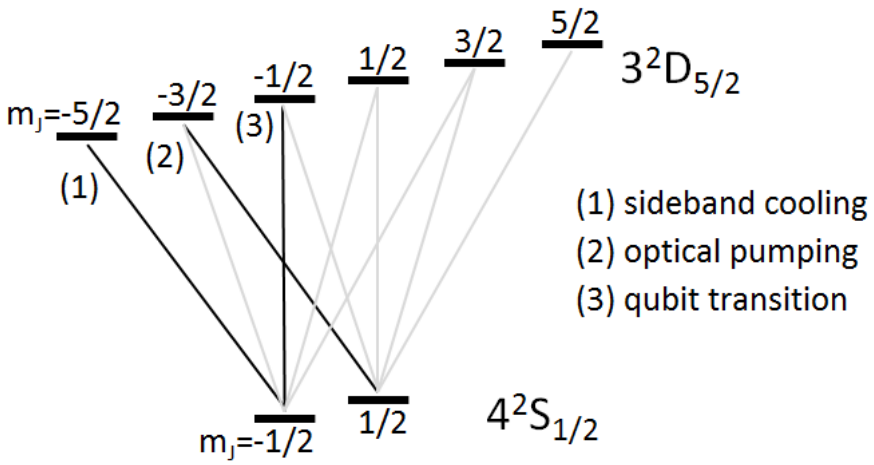


Figure 2.4: Zeeman sublevels and corresponding transitions from $4^2S_{1/2}$ to $3^2D_{5/2}$ after lifting the degeneracy. The individual transitions can be addressed by adjusting the wavelength and polarisation of the 729 nm laser. For three of them, their specific purpose during the experiment is stated.

Three of these play an important role during the experiment. To perform sideband cooling the transition $S_{1/2}(m_J = -1/2) - D_{5/2}(m_J = -5/2)$ is used. This is described in subsection 2.4.2 in more detail.

There are two possible uses for the $S_{1/2}(m_J = -1/2) - D_{5/2}(m_J = -1/2)$ transition. On the one hand it is often used to encode qubit information ($|S\rangle$ and $|D\rangle$). On the other hand one can use it to measure the motional heating rate of the trapped ions. How this is performed is described in subsection 3.2.3.

The third important transition is $S_{1/2}(m_J = 1/2) - D_{5/2}(m_J = -3/2)$. This transition, together with a repumping laser at 854 nm, collects the population in the $S_{1/2}(m_J = -1/2)$ state. This procedure is called optical pumping and acts in our case as initialising step for the experiments.

Until now, Paul traps are introduced as a tool that allows us to trap the ions in vacuum and the choice to use $^{40}Ca^+$ as a species in the described experiments is motivated. In the trap the ions are insulated from the environment and can be manipulated by lasers. The following section gives some further information about the quantum mechanical behaviour of the combined system of ion and trap.

2.3 Laser-ion interaction

This section gives the quantum mechanical description of an ion in a Paul trap. A more detailed treatment is given in ref. [14]. In the following, the ion is treated as a two-level-system with the qubit states $|S\rangle$ and $|D\rangle$ as ground state and excited state, respectively. Their energy difference is $\hbar\omega_e$. The quantized motion of an ion in the Paul trap is that of a quantum mechanical harmonic oscillator of frequency ω_T. The equidistant energy levels of the harmonic oscillator are given with $\hbar\omega_T(n + 1/2)$, where n is the phonon number associated to the Fock state $|n\rangle$. The trapped ions can interact with a laser of frequency

ω_{L}. The laser can either be used to address the transition of the qubit, $|S\rangle - |D\rangle$, or to couple the qubit with the motional state. This can be selected by adjusting the detuning of the laser, $\Delta = \omega_{\mathrm{L}} - \omega_{\mathrm{e}}$. A resonant laser only drives the qubit transition, whereas a detuning of $\Delta = \pm\omega_{\mathrm{T}}$ leads to a coupling of the electronic state to the motional state of the ion in the trap.

This quantum mechanical system can be described by a Hamiltonian, H, which consists of both, a time-dependent and a time-independent part. The description of the two-level-system, H_{e}, and the ion's motion in the trapping potential, H_{m}, make up the time-independent part, H_0. The interaction between ion and laser is described by H_{i} and accounts for the time-dependent part:

$$H = H_0 + H_{\mathrm{i}} = H_{\mathrm{m}} + H_{\mathrm{e}} + H_{\mathrm{i}}. \tag{2.13}$$

The Hamiltonian of the two-level system can either be written as

$$H_{\mathrm{e}} = \hbar\frac{\omega_{\mathrm{e}}}{2}(|S\rangle\langle S| - |D\rangle\langle D|), \tag{2.14}$$

or, by using spin-1/2 algebra and the Pauli spin matrices, as

$$H_{\mathrm{e}} = \hbar\frac{\omega_{\mathrm{e}}}{2}\sigma_{\mathrm{z}}. \tag{2.15}$$

The motional Hamiltonian consists of the potential and kinetic energy of the ion in the harmonic potential. The usual notation replaces the displacement x and the momentum p of the ion by the corresponding operators $\hat{x}$ and $\hat{p}$. Therefore, the Hamiltonian can be written as

$$H_{\mathrm{m}} = \frac{\hat{p}^2}{2m} + \frac{m\omega_{\mathrm{T}}^2\hat{x}^2}{2}, \tag{2.16}$$

or, by using the annihilation and creation operator a and $a^\dagger$, as

$$H_{\mathrm{m}} = \hbar\omega_{\mathrm{T}}(a^\dagger a + \frac{1}{2}). \tag{2.17}$$

Operators a and $a^\dagger$ are defined as

$$a = \sqrt{\frac{m\omega_{\mathrm{T}}}{2\hbar}}\left(\hat{x} + \frac{i\hat{p}}{m\omega_{\mathrm{T}}}\right) \tag{2.18}$$

and

$$a^\dagger = \sqrt{\frac{m\omega_{\mathrm{T}}}{2\hbar}}\left(\hat{x} - \frac{i\hat{p}}{m\omega_{\mathrm{T}}}\right), \tag{2.19}$$

respectively. The time-dependent Hamiltonian describing the interaction between the ion and a laser beam can be written as

$$H_{\mathrm{i}} = \frac{1}{2}\hbar\Omega(\sigma^{+} + \sigma^{-})(e^{i(kx-\omega_{\mathrm{L}}t+\phi)} + e^{-i(kx-\omega_{\mathrm{L}}t+\phi)}), \tag{2.20}$$

where $\sigma^{\pm} = (\sigma_{\mathrm{x}} \pm i\sigma_{\mathrm{y}})/2$ [14]. This is the one-dimensional description, for a laser beam of wave number k, which is aligned parallel to the x axis of the trap. The Rabi frequency Ω corresponds to the coupling strength between the ion and the light field. By applying a unitary transformation of the form $H_{\mathrm{I}} = U^{\dagger}H_{\mathrm{i}}U$, with $U = e^{-iH_0/\hbar}$, the Hamiltonian H_{i} can be transformed from the Schrödinger picture into the interaction picture. This transformation, together with the simplification given by the so-called rotating wave approximation, leads to an interaction Hamiltonian of the form

$$H_{\mathrm{I}} = \frac{1}{2}\hbar\Omega(\sigma^{+}e^{i\eta(\tilde{a}+\tilde{a}^{\dagger})}e^{-i\Delta t} + \sigma^{-}e^{-i\eta(\tilde{a}+\tilde{a}^{\dagger})}e^{i\Delta t}), \tag{2.21}$$

where $\tilde{a} = ae^{-i\omega_{\mathrm{L}}t}$ and η is the Lamb-Dicke parameter. This parameter is defined as

$$\eta = k\sqrt{\frac{\hbar}{2m\omega_{\mathrm{T}}}} = kx_0, \tag{2.22}$$

where x_0 stands for the spread of the ground state wave function of the ion. The rotating wave approximation uses the fact that fast-oscillating terms have a small influence on the time evolution of the system and therefore they are neglected in this description. In the given situation, the quantum mechanical states contain two informations: On the one hand the electronic state of the ion, $|S\rangle$ or $|D\rangle$, and on the other hand the motional state of the ion in the trap described by the associated phonon number, $|n\rangle$. Equation 2.21 describes the possible coupling between the ground state and the excited state including a change of the motional state, i.e. $|S,n\rangle \leftrightarrow |D,m\rangle$ with $n \neq m$. By adjusting the detuning of the laser, one can select the states that are coupled. The coupling $|S,n\rangle \leftrightarrow |D,m\rangle$ requires a detuning of $\Delta \approx (m-n)\omega_{\mathrm{T}}$. Depending on the detuning, three types of transitions can be distinguished. The case $m = n$, i.e. no change in the motional state, is called a carrier transformation, whereas for $n < m$ and $n > m$ the transition is called a blue and red sideband transition, respectively. These different transitions are shown in figure 2.5.

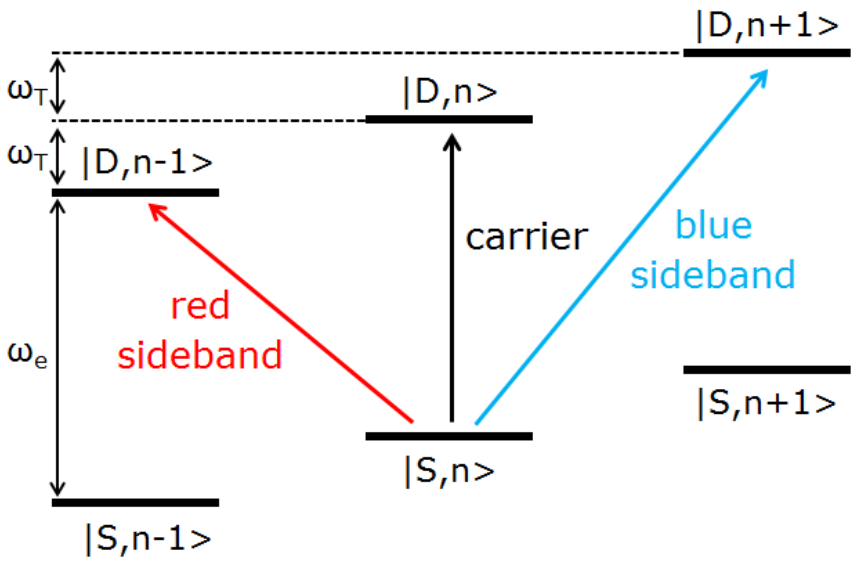


Figure 2.5: Carrier transition and first-order sidebands of the qubit transition. The sidebands occur due to the joint consideration of the electronic state of the ion and the motional states in the harmonic potential. While a red sideband transition reduces the phonon number by one, a blue sideband increases it by one. A carrier transition changes the electronic state without changing the motional state.

The Rabi frequencies of these transitions correspond to their respective coupling strengths [32]. They are defined as

$$\Omega_{\mathrm{n,m}} = \Omega_{\mathrm{m,n}} = \Omega_0 |\langle n| e^{i\eta(\hat{a}+\hat{a}^\dagger)} |m\rangle|. \tag{2.23}$$

For sufficiently cooled ions, this expression can be simplified. In the Lamb-Dicke regime, where $\eta^2(2n+1) \ll 1$ is fulfilled, the probability of transitions that change the phonon number by more than one quantum, $|n-m| > 1$, gets so small, that they can be neglected. The Rabi frequency for a carrier transition is then given by

$$\Omega_{\mathrm{car}} = \Omega_{\mathrm{n,n}} = \Omega_0(1-\eta^2 n), \tag{2.24}$$

which states a weak dependence on the addressed motional state. For the red and blue sideband the frequencies are

$$\Omega_{\mathrm{red}} = \Omega_{\mathrm{n,n-1}} = \Omega_0 \eta\sqrt{n} \tag{2.25}$$

and

$$\Omega_{\mathrm{blue}} = \Omega_{\mathrm{n,n+1}} = \Omega_0 \eta\sqrt{n+1}, \tag{2.26}$$

respectively. Since the Rabi frequency is a function of the phonon number, it can be used to measure the motional excitation. A more detailed description of how this is done during the experiment, is given in subsection 3.2.3.

2.4 Laser cooling and detection

With these equations, we have a tool to describe the complete quantum mechanical system consisting of the trapped ion and the laser. An important figure for the experiments is the motional heating rate. In the described experiments, this is measured by motional sideband spectroscopy [33]. During this process, the ion is cooled close to its motional ground state. After a variable waiting time, where the cooling is switched off, the motional sidebands of the qubit transition are probed and the mean phonon number is determined. The heating rate can then be measured by varying the waiting time (see subsection 3.2.3).

Motional sideband spectroscopy can achieve a resolution of < 0.1 phonons for an ion which is cooled near to its motional ground state. For this purpose two laser cooling methods are used. As the first step, Doppler cooling is used to bring the ion into the Lamb-Dicke regime [34]. The second step is to use sideband cooling to cool further. These two methods use different atomic transitions. While the transition for Doppler cooling has a natural linewidth that is larger than the trap frequency, $\Gamma \gg \omega_\mathrm{T}$, the situation for sideband cooling is the other way round, i.e. $\Gamma \ll \omega_\mathrm{T}$. Therefore it is mentioned, that Doppler cooling takes place in the unresolved-sideband or weak-binding regime, while sideband cooling happens in the resolved-sideband or strong-binding regime. The upcoming subsections give a short description of the cooling and detection steps, while all the details can be found elsewhere [32].

2.4.1 Doppler cooling

The amount of photons that an ion can scatter during one oscillation in the trapping potential in the weak-binding regime, is relatively high. These oscillations lead to a periodically alternating velocity and thereby to a time-dependent Doppler shift. This shift affects the photon scattering rate and makes it also oscillating in time. While the momentum transfer of an absorbed photon is always along the laser direction, the direction of the momentum transfer of emitted photons is random. This randomness leads to a vanishing average momentum transfer. Therefore, a laser beam can create a velocity-dependent pressure, which cools the ion when red-detuned light is used and that heats the ion for blue detuned light. Due to the constant change of absorption and emission, the minimum achievable momentum of the ion is limited (Doppler limit) [34]. For a detuning of $\Delta = -\Gamma/2$, the minimum energy of the ion, reachable by Doppler cooling is given by

$$E_\mathrm{D} = \frac{\hbar\Gamma}{2}, \tag{2.27}$$

which corresponds to a minimum mean phonon number of

$$n_\mathrm{min} \approx \frac{\Gamma}{2\omega_\mathrm{T}}. \tag{2.28}$$

The typical numbers and parameters of the presented experiments, $\omega_\mathrm{T} = 2\pi \cdot 1\,\mathrm{MHz}$, $\eta = 0.07$ and the natural linewidth $\Gamma = 22.4\,\mathrm{MHz}$ of the $S_{1/2} - P_{1/2}$ transition, limit

the reachable mean phonon number to $n_{\min} \approx 11$. Therefore, the Lamb-Dicke regime, $\eta^2(2n+1) = 0.113 \ll 1$, can be reached via this method.
The efficiency of the Doppler cooling process is also limited by the overlap of the principal axes of the trap with the laser beams. The motion along one of those axes can only be cooled if the laser beam has a component parallel to the corresponding axis. This may be difficult to achieve, especially with surface ion traps where usually all laser beams need to be guided parallel to the surface. Modifications in the trap design can help to improve the cooling efficiency (see section 3.1).

2.4.2 Sideband cooling

Cooling beyond the Doppler limit is possible by using sideband cooling as a second method. The $S_{1/2} - D_{5/2}$ transition has a very small natural linewidth with respect to the trap frequencies ($\Gamma < 1\,\text{Hz}$), which brings us to the resolved-sideband regime. The red-detuned laser, $\Delta = -\omega_{\text{T}_\text{i}}$, couples the states $|S, n\rangle$ and $|D, n-1\rangle$, which reduces the corresponding phonon number by one for each cooling circle.
In order to increase the cooling rate, the metastable $D_{5/2}$ state is coupled to the short lived $P_{3/2}$ state. This is done with a repumper laser at 854 nm. The $P_{3/2}$ state predominantly decays to the S state without an additional change of the motional state. As the phonon number decreases and finally the state $|n = 0\rangle$ is reached, there is no state for the red sideband to couple to and its coupling strength vanishes. This ends the cooling process automatically and the ion remains in the motional ground state. The whole cooling procedure is schematically shown in figure 2.6.

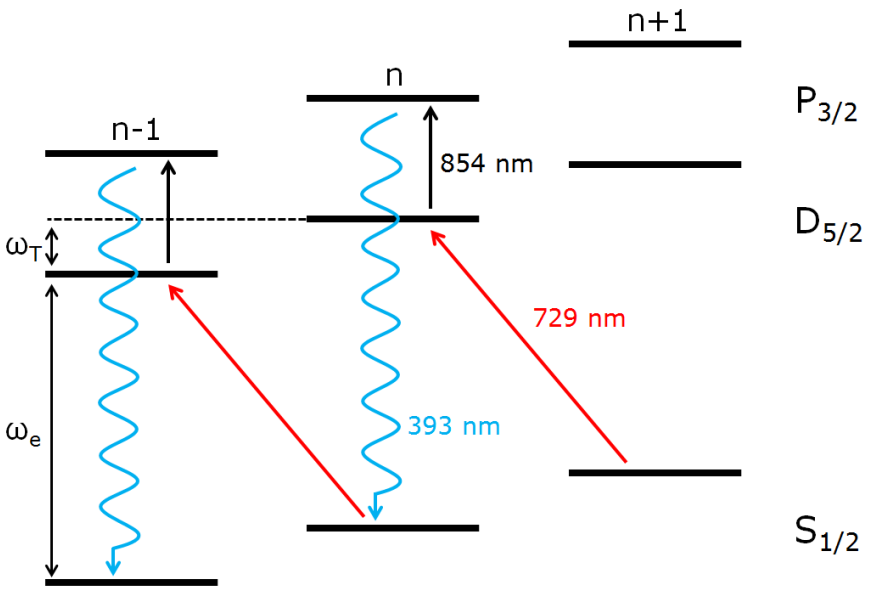


Figure 2.6: Schematic illustration of the sideband cooling procedure. The laser at 729 nm is red-detuned in order to couple $|S, n\rangle \leftrightarrow |D, n-1\rangle$. Therefore, the corresponding phonon number is reduced by one for each cooling circle. The cooling rate is increased by coupling the $|D, n-1\rangle$ state to the $|P, n-1\rangle$ state with a 854 nm laser which effectively reduces the lifetime of the D state. For sufficiently small phonon numbers (Lamb-Dicke regime), the decay from P to S happens, with high probability, without changing the phonon number.

2.4.3 State detection

The collection of the scattered photons from the $S_{1/2} - P_{1/2}$ transition is done by a photomultiplier tube (PMT) and a EMCCD camera. The scattering rate of this transition is sufficiently high to image the ion and perform a fast state detection ($\sim$ ms). In order to determine the occupation probability for the S and D states, the electron shelving technique is used. When the ion is in the S state it scatters photons due to the 397 nm laser that drives the S-P transition. No photons are scattered if the D state is occupied. This method also allows a conclusion on the occupation probabilities of the two states. This is done by repeating the measurement many times, always on the same prepared state. The electron shelving technique offers a state discrimination close to 100% [33]. It is therefore a simple and reliable way to read out the state of the qubit.

Chapter 3

Scalable ion traps for quantum computing

Since the mid-1990s, various technologies have evolved that potentially lend themselves to building a quantum computer [6,8,11]. In 2017, two quantum computing architectures were compared in a first-ever quantum computer faceoff [35]. The comparison of superconducting loops and trapped ions showed, that superconducting loops work faster, while trapped ions are more reliable. Although many of these state-of-the-art technologies look very promising, none has established itself yet.

In 1996, David Divicenzo [12] stated seven minimal requirements which are necessary to successfully build a quantum computer. His predictions are known as the *DiVincenzo Criteria*:

1. A scalable physical system with well characterized qubits
2. The ability to initialize the state of the qubits
3. Long relevant decoherence times, much longer than the gate operation time
4. A universal set of quantum gates
5. A qubit-specifc measurement capability
6. The ability to interconvert stationary and flying qubits
7. The ability to faithfully transmit flying qubits between specified locations

In principle, trapped $^{40}Ca^{+}$ ions fulfil all of these requirements. However, the scalability of trapped ions systems is given and limited by the scalability of the used traps. Existing trap designs have benefits like deep and stable trapping potentials or good optical access, but the challenge is to scale them and enable larger qubit numbers. The most promising trap architectures are segmented traps, trap arrays or modular ion traps:

Segmented traps can consist of several linear Paul traps arranged on a single chip. The individual traps form registers which are linked to each other by shuttling ions between the individual trapping sites by changing the voltages on the segmented DC electrodes [21]. For segmented traps that load a long chain of ions with equidistant spacing, the transverse

phonon modes are used to perform quantum gate operations, without the need of shuttling processes [36].

Another approach is to use an **array of individual traps** on a single chip and allow nearest neighbour interaction. Such experiments require a sufficiently small distance between the individual traps [37]. There exist already reports about successful experiments with such arrays [38, 39].

Modular ion traps may consist of individual chips. The ions in the traps on the chips form registers, which are connected via photonic interfaces. These interfaces allow to connect traps which are not on the same chip or carrier [40].

The experiments presented here operate with segmented surface ion traps fabricated on silicon substrate (see section 3.1). The second part of my thesis is about the fabrication of a novel trap design. In particular, this design allows trapping of two chains of ions and therefore building an approximate 2D array of ions. By adjusting voltages, interactions between neighbouring ions from the same chain or even between ions from different chains are possible. Simulation of the trapping potential and fabrication steps are discussed in chapters 4 and 5.

3.1 Surface ion traps

The segmented trap architecture can be realized by different trap designs. In the presented work, micro fabricated traps with segments < 1 mm in size are used. A distinction of microtraps is possible in the arrangement of their electrodes: While multi-layer traps allow a tree-dimensional arrangement of the electrodes around the ion, surface ion traps have all their electrodes in one plane. Depending on the trap, the ion levitates surrounded by or above the electrodes. These trapping situations are illustrated in figure 3.1.

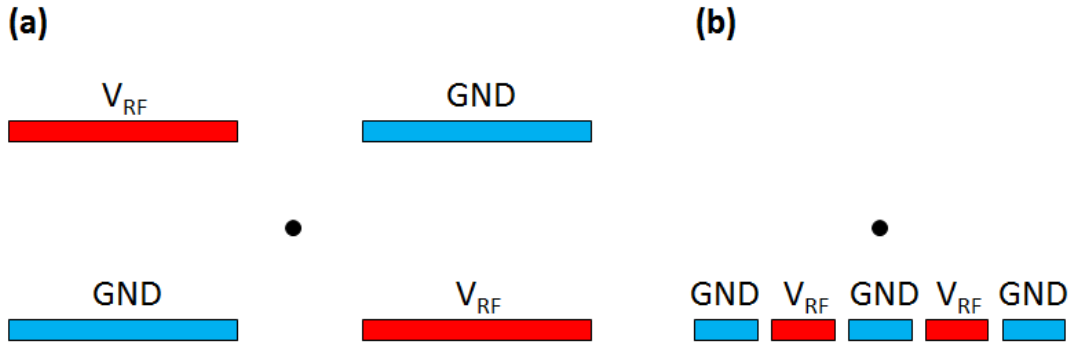


Figure 3.1: Cross section of different electrode configurations. The traps are sliced perpendicular to the trap axis. RF voltage is applied to the red electrodes and creates radial confinement(x-y plane). The blue electrodes are grounded. Black dots mark the position where the RF field vanishes, at which the ion is trapped.

These configurations have different properties: The main advantage of a three-dimensional arrangement of the electrodes around the ion is that this enables a much deeper trapping

potential than for a surface trap. On the other hand the fabrication of surface traps is usually easier and faster.

The operation principle of a surface ion trap can best be understood by looking at the typical electrode arrangement of such a trap. Starting from a traditional linear, three-dimensional Paul trap, a planar approach is achieved by splitting the top ground electrode and projecting the result onto a plane, as shown in figure 3.2.a. This gives two long RF electrodes, arranged parallel, with a grounded electrode of the same length in between. Besides each RF electrode there are segmented DC electrodes (see figure 3.2.b). The RF electrodes create the pseudopotential and therefore the radial confinement (x-y plane), while the DC segments generate the axial confinement along z. The segments together with the grounded electrode in the center are also used to keep the ion trapped at the position where the RF field vanishes. This spacial correction is called micromotion compensation.

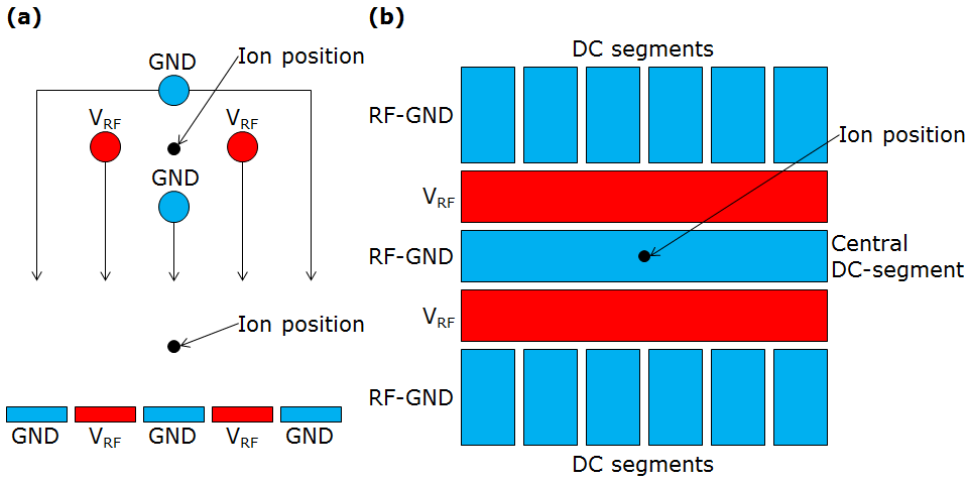


Figure 3.2: Typical electrode arrangement of surface ion traps. **(a)** Starting from a traditional linear, three-dimensional Paul trap, the top ground electrode is split and the result is projected onto a plane. **(b)** The long RF electrodes create the pseudopotential. The outer segments and the center electrode, whose RF potential is ground, are used for axial confinement and micromotion compensation.

The first experimental tests with surface traps were done in 2006 at NIST [41]. They used a quartz substrate and a structured gold layer on top formed the electrodes. Since then, many approaches where made to improve the trap performance. Among others, the substrate, the electrode material and the thicknesses of the electrodes and substrate were changed [42, 43]. Some of the latest fabrications use silicon as a substrate [44].

To use silicon as a substrate has several advantages: First to mention here is the reliability of the fabrication processes. Lithography steps and etching techniques have evolved over the last years and are the main tools to fabricate today's semiconductors. The high reproducibility meets perfectly with the requirements of ion trap fabrication. On the other hand, this opens the door towards integrated electronic components on the chip, as CMOS technology could be implemented. This would allow me to integrate filters or switches, which would reduce the number of supply lines necessary to operate the trap. Besides the integration of electronics, an integration of optics is possible. Integrated optical waveguides or micro-mirrors could be used to improve and simplify the addressing of the individual

ions. The traps used in the shown experiments are surface traps made on a silicon substrate. Different electrode configurations for surface traps are depicted in figure 3.3.

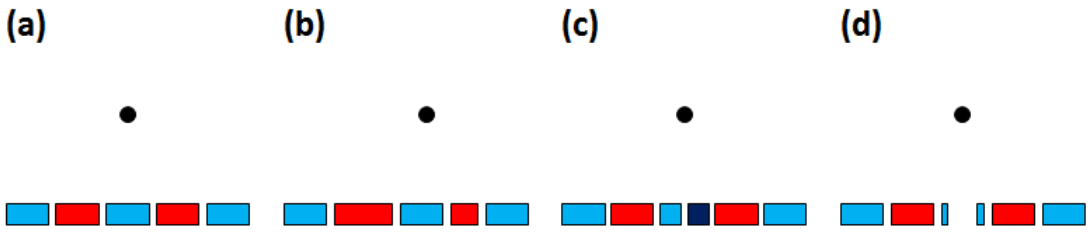


Figure 3.3: Cross section of different electrode configurations. The traps are sliced perpendicular to the trap axis. The ion position is marked by the black circles. **(a)** Symmetric trap designs typically leave one axis perpendicular to the surface. The associated motional mode has no overlap with a laser beam parallel to the surface. This issue can be resolved by applying a suitable DC potential to tilt the axes. **(b)** The asymmetric RF tilts the orientation of the quadrupole which results in a tilt of the motional modes once the DC voltages are applied. The radial principal axes are tilted with respect to the x and y direction **(c)** Applying different voltages on a split central DC electrode rotates the principal axes which makes the radial modes addressable by lasers parallel to the trap surface. **(d)** A through wafer slit in the middle of the center electrode allows me to shine laser beams perpendicular to the surface.

In spite of several advantages of surface ion traps, there are still open challenges like for example addressing and cooling of all motional modes: In order to avoid stray light from the surface, all laser beams are typically aligned parallel to it. This, in turn, makes it impossible to cool the motional mode perpendicular to the surface. This situation is illustrated in figure 3.3.a. To overcome this problem, the principal axes of the trap can be rotated. There are possibilities to reach this: One way is to apply a suitable DC potential to tilt the axes. Alternatively one can use an adapted trap design, where the RF electrodes differ in width [45]. This asymmetry leads to a rotation of the trapping potential which is noticeable once the DC voltages for axial confinement are applied. Thus, none of the principal axes are normal to the surface. The traps presented in this thesis use this solution. As a third option the central DC electrode can be split up into two individual ones [46]. By applying different voltages at these electrodes, the axes are also rotated. These two situations are shown in figure 3.3.b and 3.3.c, respectively. Without rotating the axes, one could have a slot through the wafer in the middle of the center electrode [47]. This is shown in figure 3.3.d and would enable a laser beam perpendicular to the surface without stray light. Additionally this could be used to load the trap from the backside. Loading from the back would reduce the amount of calcium atoms and residuals that hit the traps surface which in turn helps to keep the electrodes as clean as possible.

3.2 Motional heating rates

In the experiments described, the ion traps are operated in a cryostat in ultra-high vacuum to best shield the ions from the environment (see section 6.1). This is necessary because

one wants to avoid interactions with background gases. Such interactions would cause decoherence and the ions would gain kinetic energy much too quickly which would harm the experiments. The increase in energy is called heating, which corresponds to a steady increase of the mean phonon number n. Each of the motional modes can be subject to heating mechanisms. These heating rates, $\dot{n}_i$, need to be known and be kept small [47, 48]. Especially for quantum gate operations: Here, the modes of common motion, which are shared by all ions in the trap, are used to couple the electronic states and therefore the qubits. For gate operations the heating rates limit the achievable infidelities. To give some numbers, let us consider the implementation of a Molmer-Sorensen gate [49]. An infidelity of $< 10^{-3}$ is the assumed infidelity that still allows fault-tolerant quantum computing [50]. For this, the heating rate needs to be $\lesssim 100$ phonons per second.

3.2.1 Possible sources of heating

Since ions are charged particles, they are sensitive to electric fields. This is not only due to trap potentials, but also due to unwanted electrical field noise. This noise typically consists of many frequency components and is therefore described by its spectral density, $S_{\mathrm{E}}(\omega)$. The spectral components resonant with the trapping frequencies ω_{T_i} are responsible for the heating of the corresponding modes. The heating rate caused by a given spectral noise density $S_{\mathrm{E}}(\omega_{\mathrm{T}_i})$ can be calculated by

$$\dot{n}_i = \frac{Q^2}{4m\hbar\omega_{\mathrm{T}_i}} S_{\mathrm{E}}(\omega_{\mathrm{T}_i}), \tag{3.1}$$

where m and Q are the mass and the charge of the ion and ω_{T_i} are the corresponding trap frequencies with $i \in \{x, y, z\}$ [48, 51].

Adding to the example of the implementation of a Molmer-Sorensen gate, where a heating rate of $\lesssim 100$ phonons per second is required, let's calculate the maximum allowed spectral noise density. For a $^{40}\mathrm{Ca}^+$ ion trapped in a harmonic potential, $\omega_{\mathrm{T}_i} \simeq 2\pi \times 1\,\mathrm{MHz}$, the spectral density needs to be $< 10^{-12}\ \mathrm{V}^2/(\mathrm{m}^2\mathrm{Hz})$. The observed level of noise at the position of the ion can be significantly higher, as many sources contribute to it [48]. These sources have each their characteristic scaling with frequency, trap size, trap geometry and temperature. Three known sources of noise are electromagnetic radiation, Johnson-Nyquist noise, technical noise and surface noise. In the following, they are briefly discussed and possibilities are shown to reduce the corresponding heating (see subsection 3.2.2).

Electromagnetic radiation

The first possible noise source is electromagnetic radiation (EMR) which consists of different frequency components. In commercial buildings, the spectral densities around the trap frequencies can be of such strength that the experiments are harmed. Especially due to power lines [52], a level of $S_{\mathrm{E}} \approx 10^{-10}\ \mathrm{V}^2/(\mathrm{m}^2\mathrm{Hz})$ can be reached [53].
Besides the interaction with the ions themselves, EMR can be picked up by the lines going

to the trap. This coupling may lead to voltage fluctuations on the electrodes, which can cause motional heating of the ion.

Johnson-Nyquist and technical noise

The charge carriers in a conductor show a permanent movement due to their thermal kinetic energy. This movement creates an electrical noise, which is referred to as Johnson-Nyquist noise [54, 55]. This kind of noise depends on the characteristic dimension D of the trap and scales with D^{-2} [48]. The corresponding spectral density can be written as

$$S_{\mathrm{E}} = \frac{4k_{\mathrm{B}}TR_{\mathrm{JN}}(\omega, T)}{D^2}, \tag{3.2}$$

where k_{B} is the Boltzmann constant, T is the temperature of the conductor and $R_{\mathrm{JN}}(\omega, T)$ is the resistance of the conductor, which itself depends on the frequency and the temperature. The resistance arises not only from the electrodes, but from the surrounding electronics as well. With this in mind, all wire bonds need to be done with high diligence and furthermore, high quality requirements are placed on the voltage sources.

Surface noise

Due to the fact that the materials of the electrodes and the substrate are not perfect, surface noise can arise [48]. In particular, different crystal orientations and grain structures in the conductor are the main sources [56]. Besides the imperfections of the material, also contaminations of the surface are critical. Charge carrier on the surface or in the substrate can fluctuate over time and thereby create noise at the position of the ion. The issues concerning surface noise are still not fully understood and are under ongoing investigation [48].

3.2.2 Reducing the heating

Depending on the heating source, there are several methods that allow me to minimize the heating. Surface noise can be reduced by using traps with pristine and clean surfaces or applying in-situ cleaning procedures with a pulsed UV laser or sputter cleaning with Ar^+ ions [57, 58]. Johnson-Nyquist noise and noise caused by EMR can be reduced by filtering the voltages and shielding of the supply lines. Additional shielding of the experimental setup protects the ion itself from EMR.

The direct interaction of the EMR with the ion can be suppressed by running the experiments in a shielded surrounding. The used vacuum chamber is made of stainless steel and offers some shielding. For additional protection, the trap can be mounted inside a Faraday cage. For this purpose a high conductive material like copper can be used [59, 60]. The supply lines are shielded cables and as short as possible. This minimizes the coupling of EMR to the wires.

Low-pass filters further reduce noise, which is on the lines, which helps to keep the DC voltages clean. Besides perturbations due to EMR, these filters also address Johnson-Nyquist noise and technical noise from the power supply and other electric devices. The filters are installed very close to the trap, in order to minimize the unfiltered cable length. Integrated filter electronics could further improve the situation.

3.2.3 Measurement of motional heating rates

The heating rate is a continuous increase of the motional excitation of one mode of the ion in the trap. It is measured in phonons per second and can be determined in different ways. One method is to investigate the temperature-dependent variation of the scattering rate of the Doppler-cooling transition [61, 62]. This measurement is relatively easy to execute, but is not practical for low heating rates. In this case, sideband spectroscopy is used to determine the heating rate.
This technique requires that the ion is initially cooled to the resolved-sideband regime (see subsection 2.4.2). After state initialisation, the cooling is interrupted for a specific waiting time, followed by an analysis pulse. The analysis laser operates at 729 nm and has a linewidth $\leq 1\,\mathrm{kHz}$. The mean phonon number, $\bar{n}$, can be determined by the sideband ratio technique, described in reference [63] and shortly discussed here: The analysis pulse drives the red or blue sideband of the qubit transition which delivers the excitation probability for the corresponding sideband pulse, $P_\mathrm{e}^\mathrm{rsb}$ or $P_\mathrm{e}^\mathrm{bsb}$. For a thermal state, the ratio of these probabilities is connected with the mean phonon number via

$$R = \frac{P_\mathrm{e}^\mathrm{rsb}}{P_\mathrm{e}^\mathrm{bsb}} = \frac{\bar{n}}{\bar{n}+1}, \tag{3.3}$$

which means that the ratio can be used to determine the mean phonon number:

$$\bar{n} = \frac{R}{1-R}. \tag{3.4}$$

The experimental used pulse sequence for sideband spectroscopy is as follows: After Doppler and sideband cooling (397 nm, 866 nm), the cooling lasers are switched off. During this period (waiting time) the ion heats up. What follows is an analysis pulse on one of the sideband transitions (729 nm). State detection and repumping to the initial state closes the circle (397 nm, 866 nm, 854 nm). Sideband spectroscopy allows to measure changes of the mean phonon number smaller than 0.1 phonons. The heating rate is obtained by measuring the mean phonon number for different waiting times and fitting it with a linear function.

Chapter 4

Trap design and simulation

The described experiments in this thesis are carried out with linear surface ion traps. The trap design, called 'Yedikule' (YK), is discussed in subsection 4.1.1. The corresponding trapping potential simulations are presented in subsection 4.1.2. However, the fabrication and experimental characterization of YK traps makes up only one part of my thesis. The second part is the implementation of a workflow and the mask design for a novel trap. The development of the design and the main simulations done by Philip Holz and will be part of his PhD thesis. My part is to assist the simulations and to implement a workflow for the fabrication. The new design is a two-dimensional linear trap array and should allow quantum simulation with a 2D lattice of trapped ions. Section 4.2 gives a short motivation for this approach, followed by a description of the trap design and the underlying simulations.

4.1 Linear traps "Yedikule"

The 'Yedikule' trap design is a segmented linear surface trap with seven DC electrodes on each side. The name originates from a Turkish fortress and prison Yedikule Hisari which means 'Fortress of the Seven Towers'. The basic design is not new, but was already used by a former PhD student of the group, Michael Niedermayr [23]. Different variations of the YK design are fabricated during my thesis. The reuse of the design gives us the opportunity to compare the fabrication by the FH Vorarlberg, who fabricated YK traps in 2012, and the fabrication by Infineon Technologies in Villach. A second aspect of this choice is that it was thought to be good first step into the cooperation between the University of Innsbruck and Infineon Technologies with a relatively high probability of successful trapping.

4.1.1 Trap geometry

The basic YK geometry is shown in 4.1, together with the definition of the coordinate system used in this thesis. The RF electrode surrounds a central DC electrode, labelled as C1. The seven DC electrodes on each side are referred to as L1-L7 (R1-R7). The coordinate system is chosen such that the z axis is parallel to the central electrode and is

therefore directed along the trap axis. The axes x and y are called radial axes, where x (y) is directed parallel (perpendicular) to the trap surface. Due to the geometry of the RF electrode, the pseudopotential has a weak component along the trap axis which causes a small amount of axial micromotion. This effect can be mitigated by extending the length of the RF electrode. From the simulations we see that the trapping position along the axis is shifted by ≤ 1 fm away from the center and therefore this effect is negligible small for all experiments reported in this thesis. As the central DC electrode is slightly shifted in the x direction from the center of the RF electrode, the trap is called asymmetric. The asymmetric RF tilts the orientation of the quadrupole, but without DC confinement, the radial modes are degenerated and no tilt can be defined. The tilt of the motional modes arises once the DC voltages are applied and the radial principal axes are tilted with respect to the x and y direction. This allows all motional modes to be addressed and cooled by the laser beams propagating parallel to the trap surface.

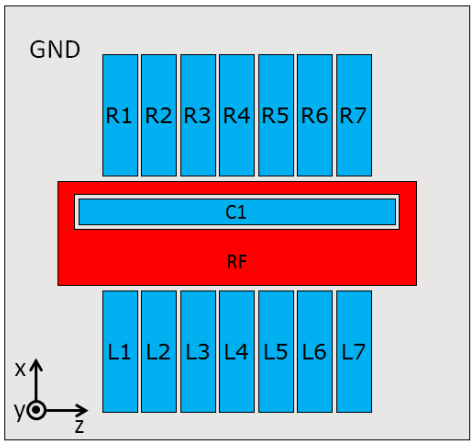


Figure 4.1: Basic geometry of the YK design and coordinate system. Radial confinement (x-y-plane) is achieved by applying an RF voltage to the RF electrode (red). DC voltages applied to the outer DC fingers (L1-L7 and R1-R7, blue) and the central electrode (C1, blue) allow axial confinement and micromotion compensation. The remaining surface of the chip is also covered with metal and is kept at ground potential (GND, grey).

During my thesis, eight variations of this basic design where fabricated, each with different electrode dimensions or gap sizes between the electrodes. The corresponding details for the individual versions are given in table 4.1. The versions differ in the gap size between the electrodes, the width of the DC fingers and central DC electrode and the asymmetry. The latter is given by the two widths of the RF electrode left and right of the central electrode. The trapping height, i.e. electrode-ion distance, is defined by the width of the RF electrodes and central DC electrode. For this reason the versions have different trapping heights of 230 µm, 150 µm, 100 µm and 50 µm, respectively.

version number	trapping height (µm)	DC finger width (µm)	central DC width (µm)	RF widths (asymmetry) (µm)		gap width (µm)
1 and 2	230	350	250	400	200	10
3	150	240	165	260	130	15
4						10
5	100	150	105	170	85	15
6						10
7	50	60	50	80	40	10
8						5

Table 4.1: Dimensions of the eight different versions of the Yedikule design. Version two is identical to version one, apart from a slit in the central DC electrode. The width of this slit is 90 µm.

Gold bonding wires with a diameter of 25 µm connect the individual electrodes to a trap carrier. The wire bonds are placed at the outer region of the electrodes. Depending on the size of the electrode, this is done either directly on the electrode or on a bonding pad. A bonding pad is needed for versions: 1 and 2 at all electrodes except RF, 3-6 at electrode C1 and 7 and 8 for the electrodes C1 and RF.

4.1.2 Trap simulation

An essential step in the development of a trap design is to perform simulations of the trapping potential. Based on these simulations the trapping parameters can be determined and the experimental setup is then prepared accordingly. For example, one needs to know the trapping height in order to align the lasers and optics. In addition, the DC and RF voltages as well as the RF frequency must be known for a stable trap potential. There are different approaches for the simulation of a two-dimensional electrode configuration. Michael Niedermayr did his simulations based on COMSOL Multiphysics 3.4, which uses the finite element method to calculate the potentials above the surface. Additionally he used MATLAB to calculate the trapping parameters like trapping height and trap frequencies [23]. In this work a python script is used that does a numerical integration of contour integrals [64].

The calculation of the electric fields and potentials for an arbitrary ensemble of electrodes relies on solving differential equations. The complexity of these calculations can be strongly reduced if two assumptions are made [65]: The first one is to have no gaps between the individual electrodes. The second is to assume, that the electrodes extend over an infinitely large plane. With these assumptions, the potentials above the surface can be calculated faster and it can be done using a numerical approach, namely the *electrode package* [64].

This methode also neglects effects of the finite electrode thickness or dielectric properties of the substrate, which are typically small compared to those of stray fields or imperfect micro-fabrication [66]. We use the *electrode package*, programmed by Robert Jördens in Python, which uses the assumptions mentioned above. For the following description of the code, the software functions are written in *italic*.

Within the *electrode package* the electrodes are represented by polygons. As mentioned before the electrodes are not separated by gaps. For this reason the size of the two electrodes next to a gap is increased such that each electrode fills up half of the gap space. The polygon vertices need to be given in a counterclockwise order. This is necessary so that the sign of the applied voltage is not inverted in the simulations. The implemented electrode layout can be plotted which delivers a picture as shown in figure 4.2. For this plot the color code refers to an arbitrary set of DC and RF voltages assigned to the electrodes. The necessary voltages for trapping are not calculated at this point. This picture is used to check that the entered polygon vertices are correct which can be seen as there is no overlap of adjacent electrodes or spaces between two electrodes.

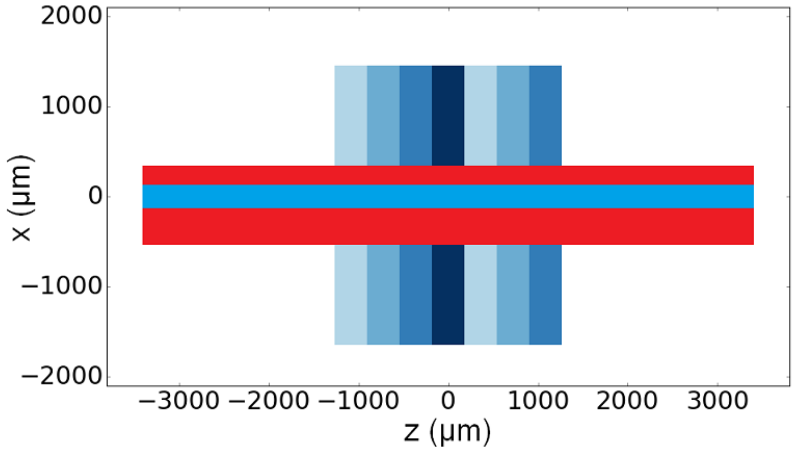


Figure 4.2: Implemented electrode layout plotted using *System.plot*. Shown are the RF (red) and the DC electrodes (blue colors). The color code represents an arbitrary set of DC and RF voltages which are applied. This picture is used to check that the polygon vertices are entered properly which can be seen as there is no overlap of adjacent electrodes or spaces between two electrodes.

After the implementation of the electrode layout the next step is to determine the pseudopotential. For this purpose, the RF voltage is assigned and the potential above the surface is calculated. In order to get the actual pseudopotential which traps the ion in radial direction, the calculated potential has to be scaled by the factor $Q^2/(4m\Omega_{\mathrm{RF}}^2)$ (see equation 2.11). The minimum of the pseudopotential can be determined by using the pre defined function *System.minimum* that looks for a minimum of the potential starting from a given start coordinate [64]. An important property to know is how much energy the ion can gain without leaving the trap. This energy can be determined by searching the saddle point of the pseudopotential and calculating the energy-difference between the saddle point and the minimum and is called trap-depth. The saddle point can be found by using the pre defined function *System.saddle* that looks for a saddle point of the potential starting from a given start coordinate [64]. Figure 4.3 shows an output of a simulation with a peak value for the RF voltage of $V_{\mathrm{RF}} = 166\,\mathrm{V}$ and $\Omega_{\mathrm{RF}} = 2\pi \cdot 20.6\,\mathrm{MHz}$. The pseudopotential confines the ion in radial direction (x-y-plane). The two cross-sections go through the calculated minimum and show the total potential above the surface. In the x-y cross section the radial confinement can be seen, whereas the z-y cross section shows that the pseudopotential does not provide axial confinement. The origin of the coordinate system is

in the center of the trap at the trap's surface. The line-plot represents the potential along the path through the calculated minimum at (41.13; 225.07; 0.00) µm and the saddle point at (60.1; 421; −8.08;) µm. This path is illustrated in the x-y cross section as red dashed line and the angle between the path and the y axis is $\varphi = 5.53°$. The trap-depth in this case is 120 meV.

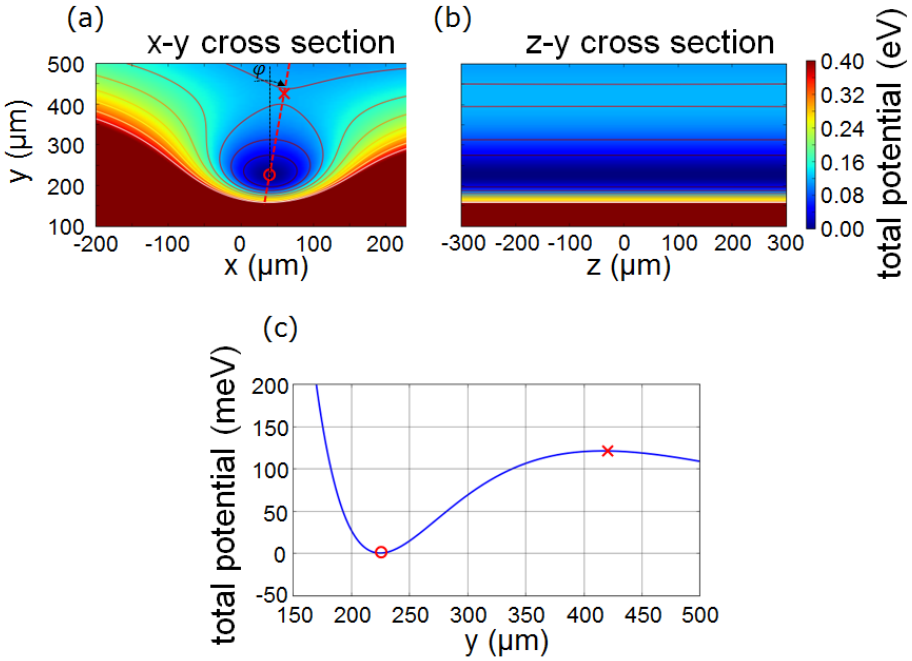


Figure 4.3: Output of a simulation of the YK design with RF voltages for radial confinement. The RF voltage is chosen to be $V_{\mathrm{RF}} = 166\,\mathrm{V}$ and $\Omega_{\mathrm{RF}} = 20.6\,\mathrm{MHz}$. The cross sections go through the calculated minimum and show the potential above the surface. The color-scale refers to the energy in electron volts (eV) and the spacing between the isopotential lines is 40 meV. **(a)** The x-y cross section of the potential. The pseudopotential confines the ion in radial direction (x-y plane). The calculated minimum is at (41.13; 225.07; 0.00) µm (red circle) and the saddle point at (60.1; 421; −8.08;) µm (red cross). **(b)** The z-y cross section. The pseudopotential does not provide axial confinement. **(c)** The line-plot shows the potential along the path through the calculated minimum ant the saddle point. The angle between the path (red dashed line in the x-y cross section) and the y axis (black dashed line) is $\varphi = 5.53°$. The trap-depth is given by the energy-difference between the saddle point and the minimum and is 120 meV.

To confine the ion along the trap axis one needs to apply DC voltages to the DC electrodes. A suitable set of voltages can be calculated with the pre defined function *System.shims* [64]. This function calculates voltage sets for different purposes under given constraints, which are given to the function as arguments. For example it should calculate a voltage set for axial confinement under the condition that the DC electric field should vanish at the minimum of the pseudopotential (see table 4.2). Alternatively one can compute voltage sets that result in a field with only an x-, y-, or z-component at the position of the ion. These can be used for micromotion compensation as they allow a movement of the ion in one direction without changing other trap parameters.

Electrode	C1	R1	R2	R3	R4	R5	R6	R7
DC voltage (V)	-3.62	-29	29	5.8	-29	5.8	29	-29
Electrode	-	L1	L2	L3	L4	L5	L6	L7
DC voltage (V)	-	-29	19	-29	-29	-29	19	-29

Table 4.2: Set of DC voltages for axial confinement calculated from the simulations. The corresponding secular frequencies are given in table 4.3.

The position of the trapped ion is given by the minimum of the pseudopotential which is above the center of the trap in axial direction (above electrode R4 and L4), but slightly shifted towards + x direction (closer to the electrodes marked with R). Therefore, the DC voltages are symmetric along the trap axis with respect to the R4 and L4 electrode, respectively, but they are different for the R-electrodes compared to the L-electrodes (asymmetry along x direction).

Figure 4.4 shows the total potential with the same RF setting as in 4.3, but with applied DC voltages for axial confinement. The x-y cross section shows that the radial confinement is weakened by the DC voltages and there exist now two saddle points . The saddle points are at $(-23.7;\ 285;\ 0.00)\,\mu m$ with a potential energy of 48 meV and at $(145.3;\ 263.4;\ -3.02)\,\mu m$ with a potential energy of 77 meV. The minimum did not change its position. The axial confinement can be seen in the z-y cross section. The line-plot represents the total potential along the path through the minimum and the two saddle points. This path is illustrated in the x-y cross section as red dashed line. The trap-depth is weakened by the DC voltages to a value of 48 meV.

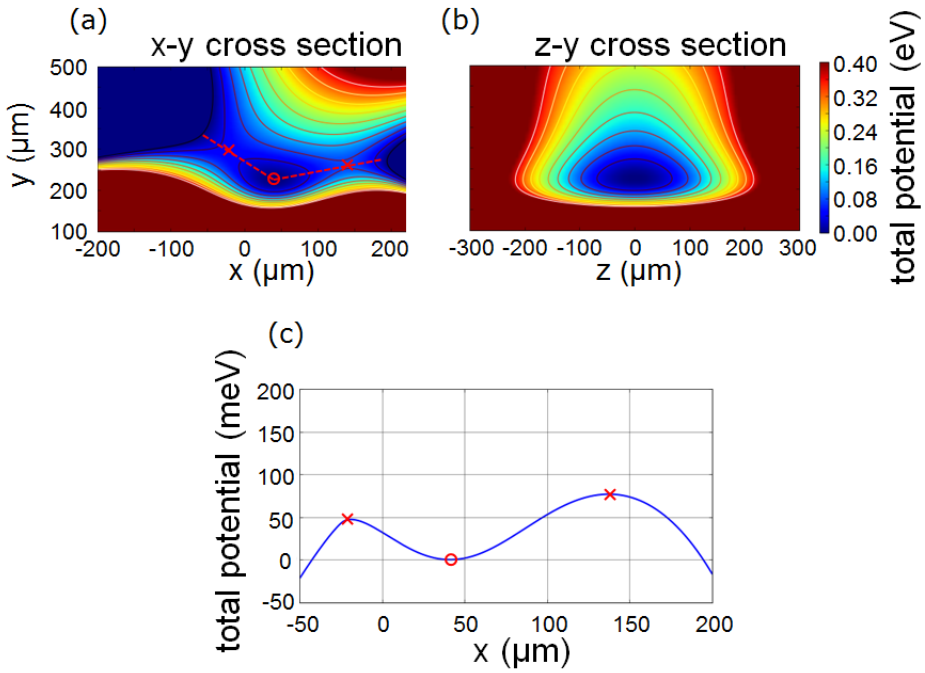


Figure 4.4: Output of a simulation of the YK design with DC and RF voltages for three-dimensional confinement. The RF voltage is chosen to be $V_{\mathrm{RF}} = 166\,\mathrm{V}$ and $\Omega_{\mathrm{RF}} = 20.6\,\mathrm{MHz}$. **(a)** The x-y cross section of the potential. The radial confinement is weakened by the DC voltages. There exist now two saddle points, one at $(-23.7;\ 285;\ 0.00)$ µm with a potential energy of 48 meV and a second at $(145.3;\ 263.4;\ -3.02)$ µm with a potential energy of 77 meV (red crosses). The minimum did not change its position (red circle). **(b)** The z-y cross section shows the axial confinement provided by the DC voltages. **(c)** The line-plot represents the potential along the path through the calculated minimum and the saddle points. This path is illustrated in the x-y cross-section (red dashed line). The trap-depth is given by the energy-difference between the lower saddle point and the minimum and is 48 meV.

An important characteristic of the trapping potential are the trap frequencies along the principal axes. As described in section 3.1, the principal axes need to be tilted in order to address and cool all motional modes with lasers which are parallel to the surface. The trap frequencies and their directions can be calculated by using the function *System.modes*. These figures are summarised in table 4.3.

$\omega_1/2\pi$	1.029 MHz	in direction	[0.000; 0.000; 1.000]	axial frequency
$\omega_2/2\pi$	1.655 MHz	in direction	[0.981; −0.195; 0.000]	first radial frequency
$\omega_3/2\pi$	1.971 MHz	in direction	[0.195; 0.981; 0.000]	second radial frequency

Table 4.3: Secular frequencies and the directions of their principal axes calculated from the simulations. The corresponding DC voltages are given in table 4.2. The axial frequency is directed along z. The principal axes of the radial frequencies are tilted by around 11° in order to address and cool all motional modes with lasers which are parallel to the surface.

It can be summarized that the deviation between the simulations made within the gapless approximation and the experiment is $< 1\,\%$ for axial frequencies (DC voltages) and $\simeq 3\,\%$ for radial frequencies (mainly RF voltage). The difference in the agreement arises from the

fact that the DC voltages are known with higher precision than the RF-voltage [67].

4.2 2D linear trap arrays

The second part of this thesis is the implementation of a workflow for a novel trap based on a design developed by Philip Holz. The details concerning the design and the simulations will be part of his PhD thesis. The idea is to build a two dimensional lattice of interacting ions to perform quantum simulations. This is realised with two parallel linear traps. The following section starts with a short motivation, followed by a description of the trap design and the underlying simulations.

4.2.1 Quantum simulation in 2D

The numerical description of a many-body quantum system is very challenging, as the dimension of the corresponding Hilbert space grows exponentially with the number of particles. Calculations become intractable even for systems involving ≈ 30 entangled particles [68]. To overcome this hurdle, Richard P. Feynman proposed to use quantum simulators instead of classical computers to perform the calculations [3]. These special purpose devices can be designed so as to give insights in specific physics problems, where classical computers reach their limits [69, 70]. Since this proposal, several experiments showed succesfully the great potential of quantum simulators [71, 72].

In order to perform a quantum simulation of a given system, one needs to define the Hamiltonian that describes the physics. Together with theorists it is then to figure out, whether it is possible to map the target problem to the qubit register and the interactions that can be performed [70, 73–75]. Essentially an ensemble of qubits with the ability to tune the coupling between the individuals is needed. In the case of two trapped ions sitting in a multi-well potential with an inter-ion distance r and a trap frequency ω, the coupling rate Ω_C is given with

$$\Omega_\mathrm{C} = \frac{e^2}{4\pi\varepsilon_0 m} \cdot \frac{1}{\omega r^3}, \tag{4.1}$$

where m is the mass of the ions, e is the elementary charge and ε_0 is the vacuum permittivity [76–78]. Therefore there are two ways to tune the coupling rate: One is to change the trap frequency, as the coupling is proportional to $1/\omega$. The second way is to shuttle the ions and vary the inter-ion distance. The coupling rate increases for lower inter-ion distance with $1/r^3$. The novel trap design of the second part of this thesis includes two linear traps on one chip where DC electrodes are used to generate a multi-well potential along the trap axes. The used electrode structure allows shuttling and formation of elementary cells of triangular or square lattices. Two parallel linear traps are the easiest case to demonstrate the shuttling and coupling. The next step could be to have more linear traps in parallel. Figure 4.5 illustrates the elementary cells and the interactions which we want

to demonstrate. Depending on the observed physical problem it is more natural to use a two dimensional architecture for the simulation (i.e. Ising model) [73–75].

Figure 4.5: Elementary cells of triangular and square lattices. The interaction, represented by the black arrows, between the individual qubits (blue balls) can be tuned by shuttling the ions against each other. The coupling rate increases for lower inter-ion distance with $1/r^3$, where r is the inter-ion distance.

4.2.2 Trap design

The presented approach to demonstrate the target shuttling operations for quantum simulation uses two parallel linear ion traps. The two traps share one RF electrode and each of them allows us to trap a chain of ions. Segmented DC electrodes provide eleven individual trapping sites per linear trap. A schematic of the trap design is shown in figure 4.6. The fact to have individual trapping sites is very important. During the experiments we want to bring ions close to each other, $\simeq 50\,\mu m$ inter-ion distance, to couple them. In order to have a reasonable barrier hight of $\simeq 2\,meV$ between two ions, individual trapping sites formed by DC voltages are advantageous.

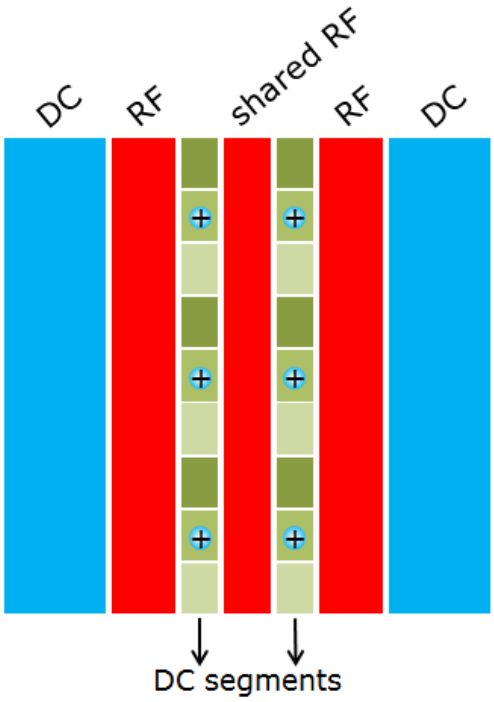
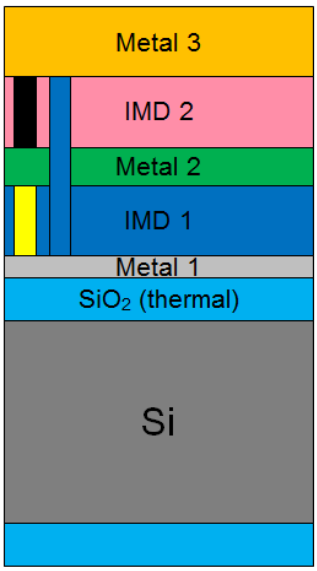


Figure 4.6: Schematic of the trap design. The trap is composed of two linear traps that share one RF electrode. DC segments provide trapping sites along the axes. The color code refers to individual voltages applied to the electrodes. The trapping positions of the ions is indicated by the blue balls marked with crosses.

The segmentation of the electrodes entails island-like electrodes and therefore a chip design with three structured metal layers and vias is used. Silicon oxide acts as an insulator between the metal layers. Figure 4.7 describes the individual layers, their thicknesses and the used materials are stated. The silicon substrate (dark grey) is covered by thermal oxide (light blue). The three metal layers are counted from bottom to top according to the order of deposition (light grey, green, orange). The inter-metal dielectric (IMD) layers are made of deposited oxide (dark blue, pink). The design contains vias, represented by the rectangles that connect the metal layers (yellow, black, dark blue). The vias are openings in the oxide, formed by etching and filled with metal. The table on the right hand side summarises the thicknesses of the layers and the corresponding materials.



Layer	Material	Thickness (nm)
Metal 3	AlSiCu	2000
IMD 2	SiO_2 (deposited)	2200
Metal 2	AlSiCu / TiN	1000 / 25
IMD 1	SiO_2 (deposited)	2200
Metal 1	AlSiCu / TiN	750 / 25
---	SiO_2 (thermal)	1300

Figure 4.7: Description of the individual layers used to fabricate the 2D trap arrays. The silicon substrate (dark grey) is covered by thermal oxide (light blue). The three metal layers are counted from bottom to top according to the order of deposition (light grey, green, orange). The inter-metal dielectric (IMD) layers are made of deposited oxide (dark blue, pink). The design contains vias, represented by the rectangles that connect the metal layers (yellow, black, dark blue). The layers thicknesses and the materials used are given in the table on the right.

The supply lines which connect the bonding pads with the electrodes are guided differently for the individual electrodes. For some lines the underlying metal layers, *metal 1* and *2* are used and the corresponding electrodes are called island electrodes. Figure 4.8 shows a schematic of the electrode structure, the wiring on the chip and the used coordinate system. As for the YK traps the z axis is again directed along the trap axis and the y axis is again perpendicular to the trap surface. The origin is chosen to be at the center of the central RF electrode, on the traps surface. The design contains several DC electrodes (*1, 2, 3, 4, A, B, C, D*) where only electrodes marked as *D* are not island electrodes. The electrodes *A, B* and *C* are smaller in size. The supply lines for the island electrodes are typically routed on *metal 2* (green lines). In the case of electrodes *A, B, C* the supply lines need to pass underneath the outer RF electrodes. In order to protect these wires from picking up RF while passing, the wires are realised using *metal 1* (red lines). Additionally the design includes a grounded plate in *metal 2* between the lines and the RF electrode. This plate is grounded by connecting it to the grounded area of the *metal 1* layer using a via between *metal 1* and *2* (yellow rectangular). Beside these supply lines, the *metal 1* layer is not structured and has ground potential. This metal layer is thought to protect the substrate from stray light. The grounding is achieved by vias connecting *metal 1* and *3* in the bonding area (vias in dark blue, marked as GND). The electrodes of the two linear traps can be addressed independently. Also the upper and lower regions of the traps are independent of each other. This provides the necessary experimental control of the individual ions for shuttling operations and micromotion compensation.

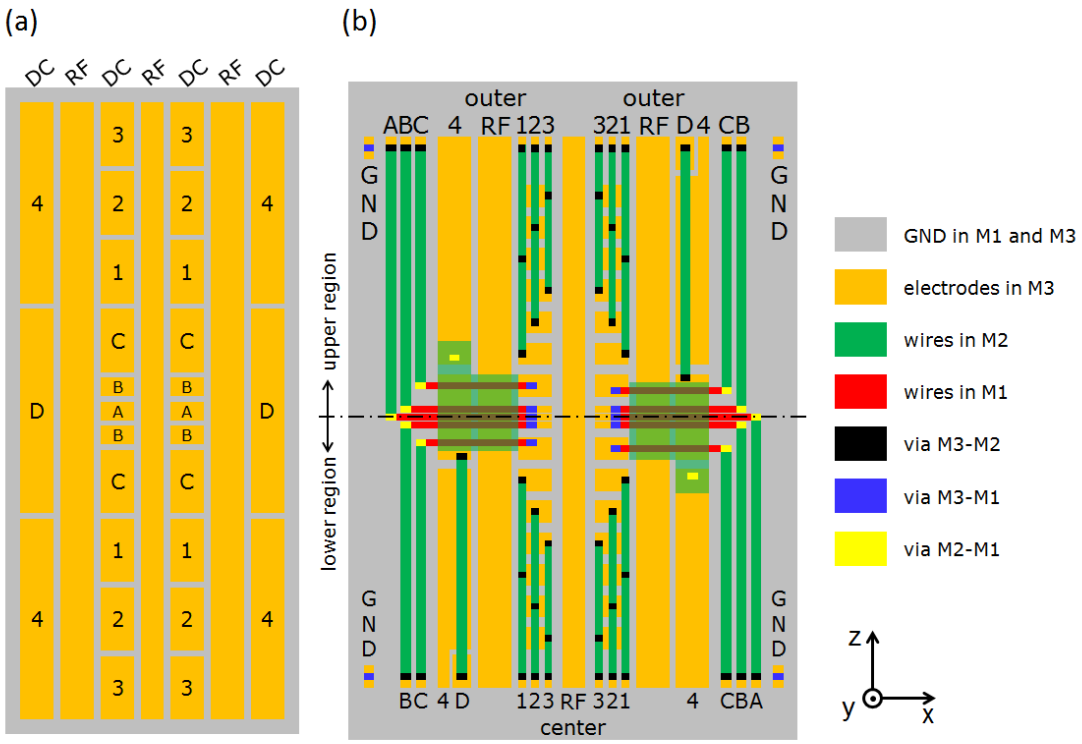


Figure 4.8: Schematic of the electrode structure and the wiring of the 2D trap arrays. **(a)** Surface electrodes of the final chip (orange). The radial confinement for two chains of ions is provided by three RF electrodes where the chains share the central one. The axial confinement is generated by the DC electrodes (*1, 2, 3, 4, A, B, C, D*). The gray area represents GND potential in *metal 1* and *3*. **(b)** Wiring of the electrodes. The supply lines which connect the bonding pads with the electrodes are partially realised by using the underlying metal layers, *metal 1* and *2*. Electrodes that have their supply lines routed on an underlying metal layer are called island electrodes (*1, 2, 3, 4, A, B, C*). In the case of the smaller DC islands *A, B, C*, the *metal 1* layer is used to pass underneath the RF electrode (red lines). To protect these wires from picking up RF while passing, the design includes a grounded *metal 2* plate between the lines and the RF electrode. This plate is grounded via a connection to the *metal 1* layer (vias in yellow). At all other areas on the chip the *metal 1* layer is not structured and has ground potential. The grounding is achieved by vias connecting *metal 1* and *3* in the bonding area (vias in dark blue, marked as GND). The electrodes of the two linear traps can be addressed independently. Moreover, are the upper and lower regions, separated by the dash-dotted line, are independent of each other. The used coordinate system is given in the lower right of the figure.

The real design contains more DC islands than shown here: Each linear trap has ten electrodes *1, 2, 3* which make together with the electrodes *A, B* (two times), *C* (two times), *4* and *D* a total of 37 DC electrodes per linear trap. Due to the electric wiring on the chip, every DC island from the upper or lower region of the liner trap that is marked with the same number is connected with each other. This periodicity reduces the amount of DC voltages needed to operate the trap. As a negative aspect this wiring leads to a possible strong RF pick-up at the electrodes *1, 2, 3*: The effective area of these electrodes that faces the RF electrode is five times bigger than for the single electrode *C*. To address this problem we fabricate different versions of the shown design, some contain less DC islands. Additionally, our versions provide two different trapping heights and different

capacities. The capacitance of the traps is varied by structuring or not structuring *metal 1* underneath the RF electrodes. The dimensions and details of the different versions are given in table 4.4.

electrode	width (along x) (µm)		width (along z) (µm)
4	193		2842.5
D	193		297
outer RF	218	243	6000
1, 2, 3, C	43	93	93
A, B	43	93	25
RF center	68	64	6000
trapping height (µm)	80	120	

Table 4.4: Electrode dimensions and corresponding trapping heights. The versions differ in their trapping height (80 µm and 120 µm) and capacitance (24.7 pF and 12.1 pF). The gap size between the electrodes is 9 µm.

The two trapping heights covered by our versions are 80 µm and 120 µm. The difference in the trapping height is realised by varying the x-widths of the electrodes. Only the outer DC electrodes *4* and *D* remain unchanged. For the 80 µm case we have two versions, with and without a removed *metal 1* layer underneath the RF electrodes (different capacitance). These versions are called *y-80* and *y-80-no-m1*. For the 120 µm case we have four versions. Beside *y-120* and *y-120-no-m1* we have two reduced complexity versions with fewer DC islands along the chains. These versions are called *y-120-min* and *y-120-min-no-m1*. The chip size, 8000 µm along z direction and 4500 µm along x direction, is similar for all versions.

4.2.3 Simulation and optimization

Radial confinement for the two chains of ions is achieved by the three RF rails, where the central rail is shared by both linear traps. The axial confinement and minima formation along the two chains is done by the DC electrodes. As mentioned before, the design allows us to trap two chains of ions and provides eleven trapping sites per chain given by the amount of DC electrodes. The minima along the chains are formed by applying corresponding voltage sets for the electrodes *1, 2, 3, 4* and *A, B, B, C, C, D*, respectively. The chip design allows one to use the trap in two different modes of operation as shown in figure 4.9. The color code refers to the applied DC and RF voltages.

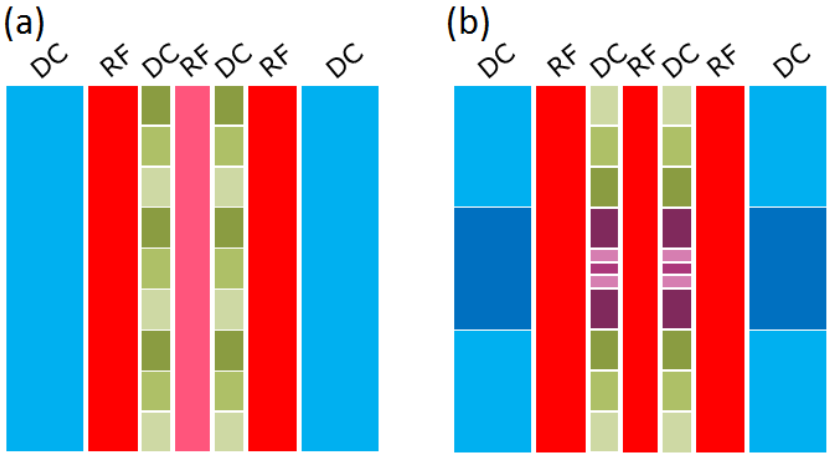


Figure 4.9: Two different modes of operation. The color code refers to the applied DC and RF voltages. **(a)** The first mode of operation. The central DC islands *A, B* and the outer DC electrodes *4, D* are each considered as one electrode. Every third DC island along the chains has the same DC voltage which produces eleven trapping sites along each chain. The amplitude at the central RF electrode can be reduced in order to bring the chains closer together. **(b)** The second mode of operation. All electrodes are treated individually, which makes the inner two minima of the chains independent of the rest of the chains. This allows us to reduce the distance of these inner minima along the trap axes.

First mode of operation: The first mode of operation is defined by the fact that the the smaller DC islands *A, B* and the outer DC electrodes *4, D* are treated as one electrode each (figure 4.9.a). The voltage set is chosen in a way that every third DC island along the chains has the same DC voltage. This allows us to load eleven sites per chain and with an attenuation of the RF amplitude at the central RF electrode the chains can be moved closer to each other.

Second mode of operation: The second mode of operation is different, as the smaller central DC islands and the outer DC electrodes are controlled individually (figure 4.9.b). As a result, the inner two minima of the chains are independent of the other minima from the chains. This enables shuttling of the central two ions from the same chain closer to each other. The simulations presented in the following use the chip either in the first or second mode of operation.

As stated in subsection 4.2.1, the use of ions for quantum simulations relies on the tunability of the coupling between the individual ions. In our approach the tuning is done by moving the ions closer to each other and change the inter-ion distance. The simulations should help to figure out, which dimensions of the electrodes give enough experimental control to perform the shuttling operations. In the first place we did so-called *electrode-width studies* in order to figure out the optimal widths of the electrodes along the x axis for radial confinement. These widths also define the trapping height. As a second task the simulations allowed us to determine the electrode widths along the z axis. Once we had two sets of electrode dimensions, referring to the two trapping heights 80 µm and 120 µm, we went on to simulate the individual shuttling operations. The details about the studies will be part of the PhD thesis of Philip Holz, who supervised my simulations. The parameters

of the RF voltage are $V_{\mathrm{RF}} = 132\,\mathrm{V}$ (root mean square) and $\Omega_{\mathrm{RF}} = 2\pi \cdot 45\,\mathrm{MHz}$. In the following, exemplary simulation results are presented that demonstrate the feasibility of the trap design. The corresponding trapping height is 80 µm.

Axial confinement

We simulate the trap in the **first mode of operation** where the smaller DC electrodes are not controlled individually. In order to get a voltage set that provides trapping sites along each chain we use, similar to the simulation of YK traps, the predefined function *System.shims*. For this simulation we define two points with minimal potential energy, one in each chain, and the function delivers a suitable set of DC voltages for their realisation. We define the minima at the center of the chains at a height where the RF field vanishes. The resulting axial confinement can be seen in figure 4.10. The two minima are at (±50.06; 77.94; 00.00) µm. Due to the periodic connection of the DC islands along the chains, each chain provides eleven trapping sites with 300 µm inter-ion distance along the trap axis. The outermost two minima at each end of the chains are affected by edge effects. For this reason, these minima are excluded from the simulations and only the inner seven are shown. The corresponding voltage set is given in table 4.5.

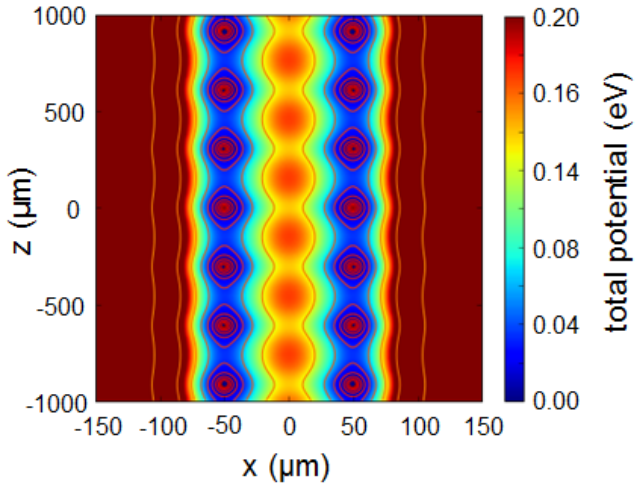


Figure 4.10: Axial confinement with seven trapping sites per chain. The chip is used in the **first mode of operation**. The RF voltage is $V_{\mathrm{RF}} = 132\,\mathrm{V}$ (root mean square) at $\Omega_{\mathrm{RF}} = 2\pi \cdot 45\,\mathrm{MHz}$. The determined minima are at (±50.06; 77.94; 00.00) µm with a periodicity of 300 µm along *z*.

Electrode	1	2	3	A	B	C	4	D
DC voltage (V)	0.90	0.50	0.90	0.90		0.50	1.33	

Table 4.5: Voltage settings for axial confinement along the trap axis. The chip is used in the **first mode of operation** as the smaller DC islands *A, B* and the outer DC electrodes *4, D* are treated as one giant electrode each. For the DC islands along the chains there are two voltages which alternate for neighbouring electrodes. The outer DC electrodes push the ions towards the center.

The voltage set for axial confinement mirrors the symmetry of the trap design. Both outer DC electrodes have the same voltage and the DC islands along the chain have two voltages which alternate. The corresponding trap frequency in axial direction (along z) is $\omega_1 = 2\pi \cdot 0.8\,\mathrm{MHz}$ and the radial frequencies are $\omega_2 = 2\pi \cdot 4.645\,\mathrm{MHz}$ and $\omega_3 = 2\pi \cdot 4.856\,\mathrm{MHz}$. The trap depth is given by different saddle points: The saddle point between two trapping sites along one chain is 34 meV, for example at (−50.00; 80.40; 153.00) µm, between the chains it is 81 meV, for example at (−0.51; 110.00; 0.00) µm and above the chains it is 110 meV, for example at (−0.04; 208.20; 0.00) µm. The inter-ion spacing along the trap axis is 300 µm and 100 µm along x. According to equation 4.1 the coupling rate for next neighbours in this configuration ($\omega_1 = 2\pi \cdot 0.8\,\mathrm{MHz}, r = 100.12\,\mu\mathrm{m}$) is $\Omega_C \approx 2\pi \cdot 109\,\mathrm{Hz}$. During the experiment such a coupling rate is too low to couple two ions with each other. Therefore this configuration is seen as coupling turned off. In addition it is possible to detune the well frequencies from each other in order to "switch off" the coupling. This could be done by changing the DC voltages of one chain and thereby changing the axial trap frequencies of the individual trapping sites with respect to those of the second chain.

Interacting chains

The next step is to simulate the case of interacting chains with the chip still in in the **first mode of operation**. The goal is to shrink the inter-ion distance to around 50 µm. For this reason we stay in the same mode as before but with changed RF settings. We increase the amplitude to $V_{\mathrm{RF}} = 200\,\mathrm{V}$ (root mean square) at the outer RF electrodes while the amplitude at the central electrode is set to 149 V (74.5 %). The outcome of the simulation is shown in figure 4.11. The calculated minima of the potential are at (±25.10; 79.50; 0.00) µm. The corresponding set of DC voltages is given in table 4.6.

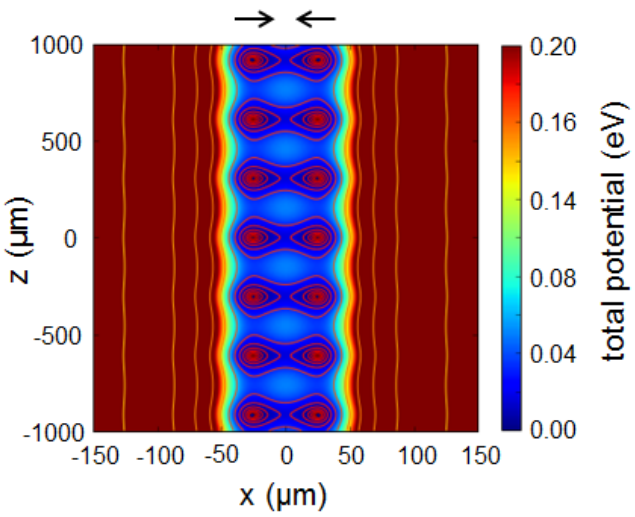


Figure 4.11: Interaction of the two chains. The chip is used in the **first mode of operation**. The RF voltage is $V_{\mathrm{RF}} = 200\,\mathrm{V}$ (root mean square) at $\Omega_{\mathrm{RF}} = 2\pi \cdot 45\,\mathrm{MHz}$. The central RF electrode has a reduced amplitude of 149 V (74.5 %). The determined minima are at (±25.10; 79.50; 00.00) µm with a periodicity of 300 µm along z. The arrows indicate the movement of the chains towards each other as a result of the lowered RF amplitude in the center.

Electrode	1	2	3	A	B	C	4	D
DC voltage (V)	0.044	0.503	0.044	0.044		0.503	0.013	

Table 4.6: Voltage settings for axial confinement along the trap axis in the case of interacting chains. The chip is used in the **first mode of operation** as the smaller DC islands *A, B* and the outer DC electrodes *4, D* are treated as one giant electrode each. For the DC islands along the chains there are two voltages which alternate for neighbouring electrodes.

The trap frequencies are $\omega_z = 2\pi \cdot 0.8\,\text{MHz}$ in axial direction and $\omega_1 = 2\pi \cdot 3.435\,\text{MHz}$ and $\omega_2 = 2\pi \cdot 3.516\,\text{MHz}$ along the radial axes. The trap depth is in this case smaller than before: Between the chains we calculate the saddle point to a value of 14 meV, for example at $(-0.253;\, 86.90;\, 0.00)\,\mu\text{m}$, along the chains it is 35 meV, for example at $(23.90;\, 84.40;\, 153.00)\,\mu\text{m}$ and above the chains it is 140 meV, for example at $(0.00;\, 224.90;\, 0.00)\,\mu\text{m}$. The inter-ion distance of $r = 50.20\,\mu\text{m}$, together with the axial trap frequency $\omega_1 = 2\pi \cdot 0.8\,\text{MHz}$ gives a coupling rate of $\Omega_C \approx 2\pi \cdot 869\,\text{Hz}$. With such a coupling rate it is possible to couple two ions from the individual chains. Therefore this configuration is seen as coupling between the chains turned on. At this point it is important to mention that the presented results only show a part of our simulations. For the experimental realisation of the shuttling operations it is also important to know about some intermediate positions between interaction turned off or on. Our simulations also included such points to confirm the feasibility of the shuttling processes.

Shuttle the chains against each other

The next important step is to simulate the shuttling of the chains against each other with the chip still in in the **first mode of operation**. This, combined with the previous shown chain interaction, would then allow us to couple one ion from the first chain with any ion from the second chain. We use the trap again in the first mode of operation and use the initial RF configuration with $V_{RF} = 132\,\text{V}$ and $\Omega_{RF} = 2\pi \cdot 45\,\text{MHz}$. The outcome of the simulation is shown in figure 4.12. The calculated minima of the potential are at $(-50.01;\, 77.90;\, -153.00)\,\mu\text{m}$ and $(50.01;\, 77.90;\, 0.00)\,\mu\text{m}$. The corresponding set of DC voltages is given in table 4.7.

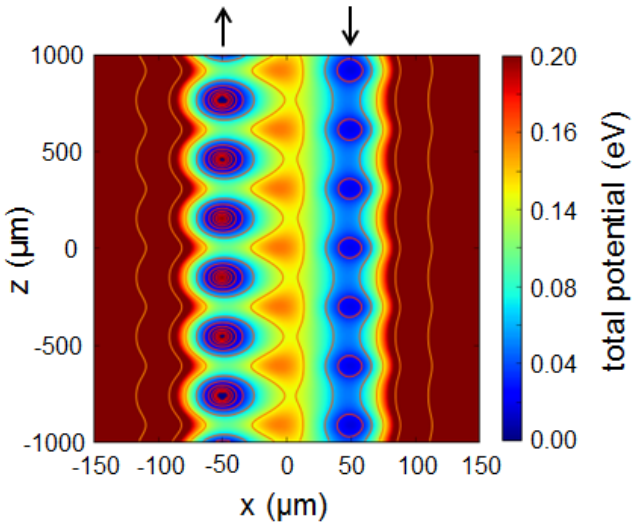


Figure 4.12: Shuttling of the chains against each other. The chip is used in the **first mode of operation**. The RF voltage is $V_{\mathrm{RF}} = 132\,\mathrm{V}$ (root mean square) at $\Omega_{\mathrm{RF}} = 2\pi \cdot 45\,\mathrm{MHz}$. The determined minima are at $(+50.01; 77.90; 00.00)\,\mu\mathrm{m}$ and at $(-50.01; 77.90; -153.00)\,\mu\mathrm{m}$ with a periodicity of 300 µm along z. The arrows indicate the mutual displacement of the two chains.

	Electrode	1	2	3	A	B	C	4	D
left chain ($x = -50$ µm	DC voltage (V)	2.59	3.89	2.59	2.59		3.89	6.47	
right chain ($x = 50$ µm	DC voltage (V)	3.11	2.52	3.11	3.11		2.52	7.12	

Table 4.7: Voltage settings for axial confinement along the trap axis with an offset in z direction for the two chains. The chip is used in the **first mode of operation** as the smaller DC islands *A, B* and the outer DC electrodes *4, D* are treated as one giant electrode each. Every chain has two DC voltages which alternate for neighbouring DC islands.

The trap frequencies are $\omega_z = 2\pi \cdot 0.8\,\mathrm{MHz}$ in axial direction and $\omega_1 = 2\pi \cdot 4.188\,\mathrm{MHz}$ and $\omega_2 = 2\pi \cdot 5.255\,\mathrm{MHz}$ along the radial axes. Between the chains we calculate the saddle point to a value of 100 meV, for example at $(4.55; 94.80; -153.00)$ µm, along the left chain it is 87 meV, for example at $(-47.7; 85.10; 0.00)$ µm, along the right chain it is 30 meV, for example at $(47.9; 80.40; 153.00)$ µm and above the chains its 210 meV, for example at $(-14.07; 256.70; -154.00)$ µm. The coupling rate in this case is again considered to be turned off and can be calculated to $\Omega_{\mathrm{C}} \approx 2\pi \cdot 19\,\mathrm{Hz}$.

Interaction of ions from the same chain

The last step is a simulation of the interaction process along the trap axes. For this purpose we use the chip in the **second mode of operation** and control the smaller electrodes individually. The RF voltage is chosen with $V_{\mathrm{RF}} = 132\,\mathrm{V}$ and $\Omega_{\mathrm{RF}} = 2\pi \cdot 45\,\mathrm{MHz}$. The outcome of the simulation is shown in figure 4.13. The calculated minima of the potential are at $(\pm 50.01;\ 77.90;\ \pm 20.00)$ µm. The corresponding set of DC voltages is given in table 4.8.

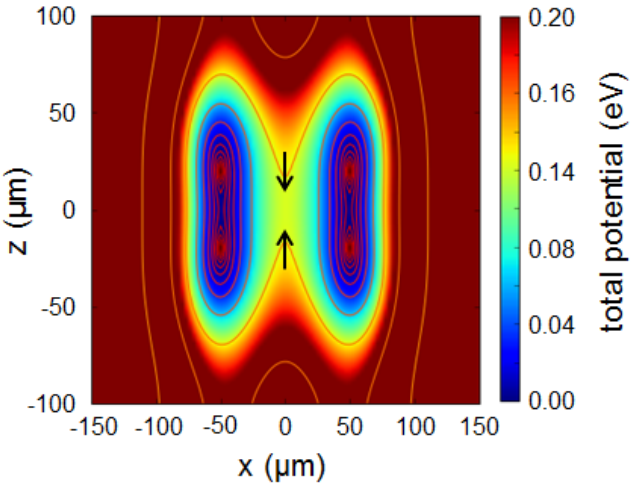


Figure 4.13: Interaction of ions from the same chain. The chip is used in the **second mode of operation**. The calculated minima are at (±50.01; 77.90; ±20.00) µm. The arrows indicate the movement of the trapping sites from the same chain towards each other.

Electrode	1	2	3	A	B	C	4	D
DC voltage (V)	0.432	0.788	1.314	8.875	-5.651	4.097	0.936	4.909

Table 4.8: Voltage set for interacting ions from the same chain. The chip is used in the **second mode of operation** as the smaller DC islands *A, B* and the outer DC electrodes *4, D* are controlled individually.

The necessary voltages for this interaction are relatively high compared to the voltage sets shown before. The barrier between the trapping sites of the same chain is 1.6 meV. The coupling rate for $\omega_z = 2\pi \cdot 1.393\,\text{MHz}$ and $r = 40.00\,\mu\text{m}$ can be calculated to $\Omega_C \approx 2\pi \cdot 987\,\text{Hz}$. The trap frequencies for the minima at $z = 20.00$ µm are $\omega_1 = 2\pi \cdot 1.393$ MHz in axial direction and $\omega_2 = 2\pi \cdot 4.506$ MHz and $\omega_3 = 2\pi \cdot 4.853$ MHz along the radial axes. For the outer minima at $z = 306.00$ µm we calculate $\omega_z = 2\pi \cdot 0.680$ MHz, $\omega_1 = 2\pi \cdot 4.586$ MHz and $\omega_2 = 2\pi \cdot 4.929$ MHz. The saddle point between the chains has a value of 73 meV, for example at (0.506; 117.00; 0.00) µm, along the chains between the not displayed minima its 90 meV, for example at (−47.80; 101.00; 80.70) µm and above the chains its 76 meV, for example at (−0.002; 156.70; 0.00) µm.

Based on these simulations it is reasonable to assume that our chip is capable to perform the presented shuttling operations during the experiments. As mentioned before, these are only some results from our simulations. We also worked on intermediate ion positions for the shuttling sequences and we calculated voltage sets for micromotion compensation of the inner most trapping sites without changing others. The simulations also include detailed information about how all trap parameters change during the entire shuttling processes, e.g. trap frequencies, axes tilt, trap depth, etc.. These details will be given in the PhD thesis of Philip Holz. The presented shuttling sequences can be combined to couple three or four ions in order to have an elementary cell of a triangular or square lattice.

Chapter 5

Fabrication of silicon traps

The following chapter describes the cleanroom facilities and the fabrication of the ion traps described in Chapter 4. The fabrication takes place at Infineon Technologies in Villach. The company's cleanroom facilities are described in section 5.1 together with a short overview of the different processes available, followed by a detailed description of the used processes to fabricate YK traps in section 5.2. Before the traps are delivered to Innsbruck, a cross section analysis and electrical tests are carried out in the failure analysis department. These results are discussed in section 5.3. Finally, after simulating and optimizing a 2D trap design, a workflow for these traps is implemented. The planned processes are summarized in section 5.4.

5.1 Cleanroom facilities

The cleanroom facilities of Infineon Technologies in Villach include roughly 23,000 square meters of cleanroom area with a chip output of around 14.3 billion chips per year [1]. The site employs about 3600 people from approximately 60 countries. Villach is considered to be the innovation factory of Infineon Technologies Austria, as evidenced by a wide variety of technologies and processes. The available wafer sizes are 4", 6", 8" and 300 mm, which results in a high level of manufacturing complexity.

5.1.1 Working in a cleanroom

In the clean room, the wafers are combined into lots, where one lot typically includes 25 or 50 wafers. All wafers need to be labelled with the corresponding lot and wafer number by means of laser scribing. The transport of the lots between the individual tools is done with boxes. For 8" and 300 mm, these boxes offer a tracking system that allows one to determine the position of the lot with an accuracy of a few centimetres. The handling of single wafers is typically done with vacuum tweezers which contact the wafer only on its unstructured backside. For very thin wafers, $\leq 140\,\mu m$, or wafers with a sensitive backside,

[1] Fiscal year 2018

edge grip tweezers are used. These tweezers grip only at the outermost edge of the wafers without damaging the structures.

Cleanrooms are distinguished by their class: The amount of particles larger than 0.5 µm, within a volume of roughly 28 dm^3 of cleanroom air, defines the corresponding class. Infineon Technologies in Villach provides cleanroom area of the classes 100 and 1000. The purity of the air is achieved by a continuous exchange of filtered air. In order to protect the cleanroom from contamination, every employee needs to wear a special cleanroom suit and gloves.

5.2 Fabrication of "Yedikule"

The fabrication of YK traps is based on the use of silicon as a substrate material. In particular we use 8" wafers as it offers the widest range of available processes compared to the other available diameters. The trap electrodes are made of gold, with an intermediate silicon oxide (SiO_2) layer between the metal and the substrate. The individual electrodes are separated by trenches.

This kind of fabrication is based on the traps made for Michael Niedermayr in 2012 by the FH Vorarlberg in Dornbirn. A schematic including a cross section of these traps is shown in figure 5.1. The 100 µm deep trenches separate the electrodes and the 2 µm SiO_2 layer acts as an insulator between substrate and electrodes. The oxide is thermally grown after etching the trenches. Thus, the side walls of the trenches are also covered with oxide. The metal layer is a stack of 2 nm titanium and 500 nm gold. The titanium acts as an adhesion promoter to avoid the gold peeling away from the surface.

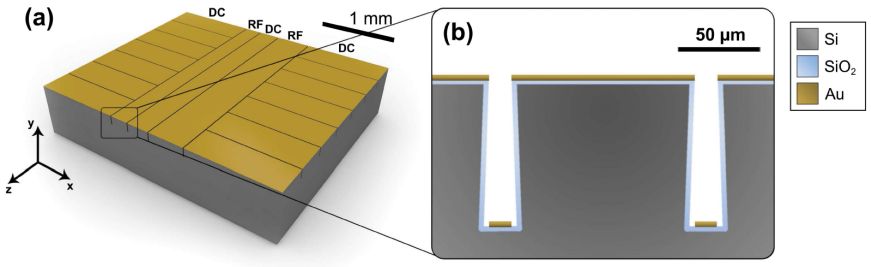


Figure 5.1: Schematic and cross section of a YK trap fabricated for Michael Niedermayr in 2012 by the FH Vorarlberg in Dornbirn. **(a)** Surface-trap design YK with a trapping height of 230 µm. **(b)** Cross section of the trap. The 100 µm deep trenches with undercuts separate the electrodes. The 2 µm SiO_2 layer insulates the substrate from the electrodes and covers the sidewalls of the trenches too. The metal layer is a stack of titanium and gold with 2 nm and 500 nm thickness, respectively. Picture taken from Michael Niedermayr's PhD thesis [23].

The process scheme that was used by the FH Vorarlberg is the following: It starts with a lithography step and deep reactive ion etching to form the trenches. The etched wafers are cleaned to remove the photo resist followed by thermal process to form the intermediate oxide layer. To separate the individual chips, laser scribing is used. The electrodes are

formed by means of gold evaporation. All these processes took place in Dornbirn, except the metallization, which was done in the university's cleanroom in Innsbruck.
In order to produce comparable traps, it is our focus to use similar processes. A short overview of the actual workflow is given here. More details about the single processes are stated in the following parts of this Chapter. A one-to-one transfer of the workflow is not possible as the fabrication in Villach does not allow one to use the oven after deep reactive ion etching due to possible contamination issues. This restriction leads to a slightly different workflow. The modified workflow starts with labelling the wafers by means of laser inscription, followed by thermal oxidation. The thermal oxide layer gets structured and the trenches are etched. The sidewalls of the trenches are covered by a deposition process. The final steps are metal evaporation and dicing. The final traps are comparable in their layers thicknesses to those made in Dornbirn in 2012. Their experimental performance is discussed and compared in chapter 7.

5.2.1 Silicon as a substrate

The choice of the substrate material includes a range of considerations. On the one hand, depending on the trap architecture and design, one needs a variety of processes available for the fabrication. The possible processes can vary for different materials, like for example for fused silica wafers. Due to their sodium content these materials are considered as critical material which reduces the range of available processes dramatically. On the other hand it is important that the substrate material does not have a negative impact on the experimental performance. Too high RF losses cause dissipation of the RF power applied to the electrodes, which heats up the chip. As the chip is part of the resonator that provides the RF voltage, heating the chip can reduce the quality factor and gain of the resonator. The lower gain forces an increase of the input RF power in order to prevent the trapping potential of getting too weak. The higher input power heats the chip even further.

The RF losses of a materials can be described by its loss tangent, $\tan\delta$, which is typically frequency dependent. In the case of an RF resonator, the loss tangent is defined as

$$\tan\delta = \frac{1}{Q_\mathrm{C}}, \text{ with } Q_\mathrm{C} = \frac{1}{R}\sqrt{\frac{L}{C}}. \tag{5.1}$$

In this equation, Q_C is the quality factor of the resonator that is given by its resistance R, capacitance C and inductance L. For materials with low RF losses, this value is $\tan\delta \ll 1$, for example fused silica has a loss tangent around 10^{-4} [79]. Fused silica would therefore be a good choice for ion trap fabrication as these losses are negligibly small. In the case of silicon the physics behind the RF losses is more complex and details are given elsewhere [80]. Without going into details: For intrinsic silicon, at the frequencies of interest for ion trapping and at room temperature, the loss tangent is proportional to

$$\tan\delta \sim \frac{\sigma}{\Omega_\mathrm{RF}\epsilon_0\epsilon_\mathrm{r}}, \tag{5.2}$$

where σ is the electric conductivity of silicon, Ω_RF is the angular RF drive frequency, ϵ_0 is the permittivity of vacuum and ϵ_r is the relative permittivity of silicon. Therefore, it

is beneficial to choose a silicon substrate with a relatively small conductivity and a high resistivity, respectively. For the fabrication of the traps in Dornbirn, intrinsic (undoped) float-zone wafers with a diameter of 100 mm were used [23]. Float-zone materials have a very high purity and therefore a high specific resistivity ρ. The specification of the wafers used in Dornbirn is $\rho > 5000\,\Omega$cm. In order to produce comparable traps, the traps fabricated at Infineon also employ float-zone silicon, p-doped with $\rho > 8000\,\Omega$cm. Even for such high specific resistivities, the loss tangent is about 1.5 for frequencies around 20 MHz, which is still far to much for a reasonable operation during experiments.

To solve this issue, one can operate silicon substrate ion traps at cryogenic temperatures. Below 25 K the charge carriers in silicon freeze out, which makes the substrate a good insulator with low RF losses [23, 80, 81]. This approach is the one taken for the YK traps. Another approach to deal with the losses of silicon is to have an additional metal layer underneath the electrodes which is grounded. This shields the substrate from the RF field [57, 82–84]. The design of the 2D linear trap arrays includes such a shielding layer.

Despite the fact that silicon imposes operational or design constraints to minimize RF losses, it also has a tremendous advantage in terms of fabrication capabilities, compared to, for example, fused silica. At Infineon Technologies in Villach, many fused silica wafers available are considered as critical material due to their sodium content. The use of such wafers would reduce the amount of available tools and processes. Additionally, there might be some issues with handling of glass wafers: some tools use electrostatic chucks where electrically insulating wafers could fall off or crack. Differences in the thermal behaviour of the substrates might alter some process conditions for fused silica wafers.

5.2.2 Thermal oxidation

Once the substrate material is chosen, the wafers are ordered and introduced to the cleanroom. After labelling and cleaning, the workflow starts with the first process, namely thermal oxidation. The thickness of the oxide layer is chosen according to two main considerations: On the one hand, it is beneficial to chose processes which are available and used for other products at Infineon Technologies. This is advantageous, as these processes are known and so they typically work without issues. Introducing new processes, like for example depositing or growing especially thick or thin layers, demands special attention and treatment from process experts. The risk of damaging wafers by, for example, cracks or wafer bow (thermal or mechanical stress) is significantly higher when using unknown processes. Even worse, chipped wafers could contaminate equipment in the cleanroom. Therefore, the use of approved processes minimizes the risk of failing and helps to speed up the fabrication. On the other hand, it is a target to stick as close as possible to the specifications of Michael Niedermayr's traps. The oxide layer of his traps is 2 µm thick.

The later deposition process that covers the sidewalls contributes to the final layers thickness. Contrary to this, the deep reactive ion etching process partially etches the SiO_2 hard mask. With this in mind, 1.3 µm thermal oxide is grown. With an expectation to lose around 400 nm while etching the trenches and a planed deposition of 2.5 µm to cover the sidewalls. This results in a final oxide layer of around 3.4 µm between the substrate and the electrodes.

5.2.3 Lithography

The next step, according to the workflow, is lithography, which is basically a combination of three steps: Coating the wafers with photo resist, exposing the resist to UV light through a photo mask and developing the resist. It is one of the most important processes in semiconductor fabrication. The correct choice of resist together with a suitable set of parameters for exposure is essential to reach the needed resolution. The photo resist is used to structure the thermal oxide layer by means of etching.

The resist is applied by spin-coating which results in a highly uniform layer thickness all over the wafer. The thickness can be adjusted by changing the speed of the spin coater. One can distinguish between positive and negative photo resist. These two polarities show different behaviour when they are exposed to UV light. For positive (negative) resist, the exposed (not exposed) parts are soluble to the photo-resist developer. Due to diffraction of the light at the slits of the mask, the slope of the resit's sidewalls is different for these two types. This is illustrated in figure 5.2.

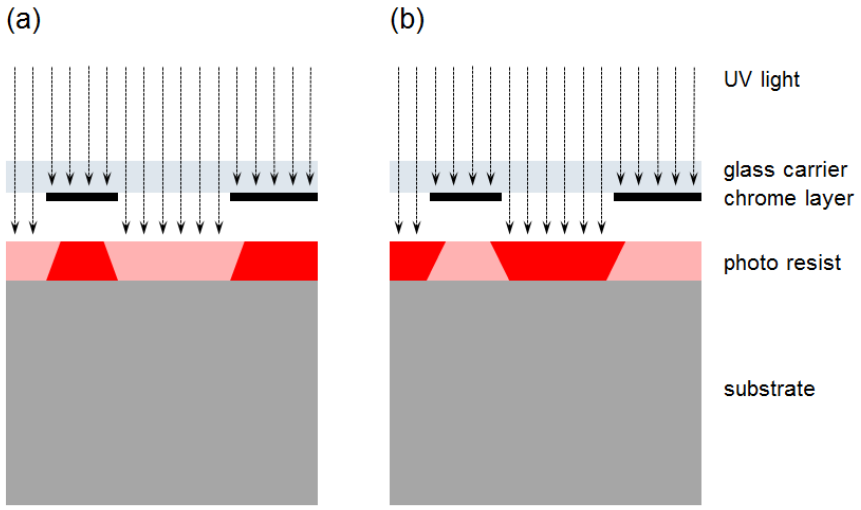


Figure 5.2: Comparison of the exposure for positive and negative resist. The substrate (grey) is coated with resist (red). The mask is a glass carrier (light gray) with a structured chrome layer (black). The UV light (dashed arrows) changes the chemistry of the resist at the exposed areas. **(a) Positive resist:** The exposed resist is weakened and can be removed during the developing process (light red). Areas where the resist should be removed get larger due to diffraction. **(b) Negative resist:** The exposed resist becomes insoluble to the photo-resist developer. Areas where the resist should remain get larger due to diffraction.

For exposure, a glass carrier with a structured chrome layer is used. It is possible to exposure the whole wafer with one exposer step (shot). In this case the glass carrier is called *mask*. As an alternative, the glass carrier can cover only a small part of the wafer with one exposer step and its structure is stepped all over the wafer using many shots. In this case the carrier is called *reticle*. The resolution limit for masks is around 2.5 µm, while for reticles this can be 50 nm. Typically, 1:1 masks are more susceptible to errors and have a shorter lifespan because they often come in contact with the wafer during the process. The reticles that contain the structures of the fabricated YK traps are presented in the

appendix 8.

All lithography steps discussed in this thesis operate with reticles. It is important to mention that the two reticles with the YK traps where not designed by me. These reticles where designed and ordered as a part of a previous project between the University of Innsbruck and Infineon Technologies. The responsible person, Herbert Weitensfelder, ordered the reticles in November 2015, but never used them.

Depending on the subsequent processes for which the lithography is made, many things have to be considered. This includes design rules for the reticles, open area of the reticle (proportion of exposed area), thickness of the resist, the polarity of the resist and accordingly the polarity of the reticle. Once these parameters are set and the reticles are designed, ordered and delivered, one needs to find suitable exposure parameters, namely focus position and dose of the UV light. The lithography parameters for stable processing are determined by a focus-exposure matrix (FEM, german: "Fokus-Dosis Staffel") where focus position and dose are varied for every shot on one wafer.

Focus-exposure matrix (FEM)

A focus-exposure matrix is an usual way to optimize the exposure for the corresponding lithography step. With reticles, it is possible to vary the exposure parameters for every shot across a single wafer. In our fabrication, one wafer contains the structure of 63 individual shots, arranged in 7 columns and 11 rows. As schematically shown in figure 5.3a, the focus position is varied from $-1.5\,\mu m$ to $1.5\,\mu m$ with an increment of $0.5\,\mu m$ and the dose from $900\,J/m^2$ to $3900\,J/m^2$ with an increment of $300\,J/m^2$. For evaluation, SEM pictures of a chosen structure with a pitch of $10\,\mu m$ are taken from each shot. The corresponding lines and spaces are analysed by image recognition to determine the optimal exposer parameters. Example SEM pictures are shown in figure 5.3b and 5.3c, with lines and spaces of $4.49\,\mu m$ and $5.57\,\mu m$ width, respectively.

With optimal processing one would expect $5\,\mu m$ each. In this case, the reticle was designed without considering the used process flow. Typically, one would choose the thickness of the layer that needs to be structured and the corresponding etching process. Once these points are fixed, the polarity and the thickness of the resist are chosen and the reticle is designed accordingly. If this is done properly, the design is transferred by the exposer process with only low deviations. In order to find the optimal lithography parameters to fabricate the YK traps, the wafer with the FEM is processed until the end of the work flow and the lines and spaces are measured after every process.

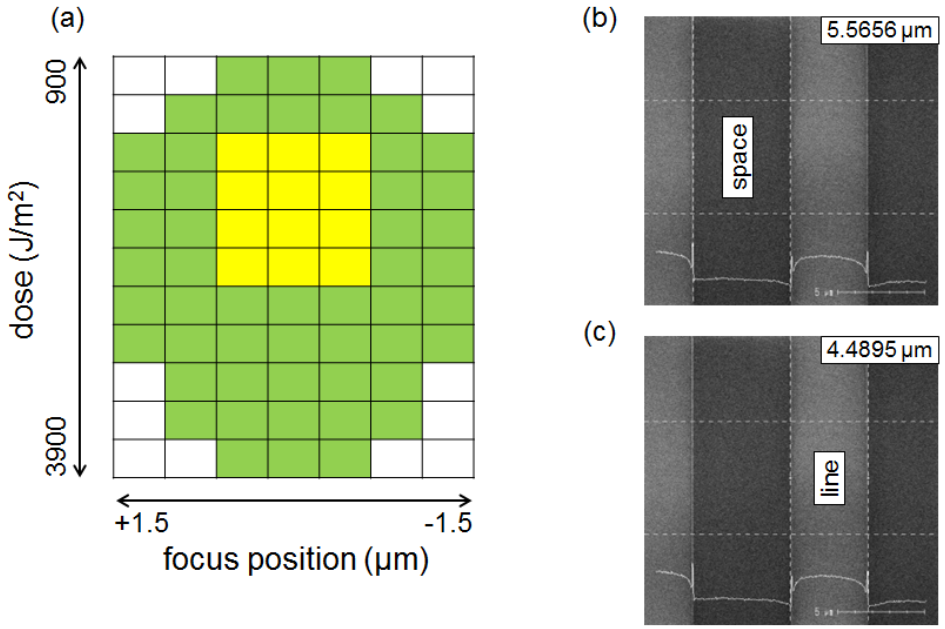


Figure 5.3: Focus-exposure matrix to optimize the exposure. **(a)** Schematic of the 63 shots on the wafer (green and yellow). The focus position is varied from $-1.5\,\mu m$ to $1.5\,\mu m$ and the dose from $900\,J/m^2$ to $3900\,J/m^2$. **(b)** and **(c)** Example SEM pictures for the evaluation, taken from structures with lines and spaces of $5\,\mu m$ each. The width of the lines and spaces is measured and analysed by image recognition. The shown lines and spaces have a width of $4.49\,\mu m$ and $5.57\,\mu m$, respectively. As a result, the lithography parameters for stable processing are identified (shots in yellow).

As a result, it is possible to identify the lithography parameters for which the lithography process is considered to be stable and, moreover, the final dimensions of the traps are as similar as possible to the actual design. It turns out that the actual trenches are about $1\,\mu m$ wider than intended in the design. The reason for this is that the reticle was designed without a target process flow. The selected process sequence consisting of thermal oxidation, lithography, wet-chemical etching of the oxide and plasma etching of the substrate can only image this reticle with a deviation of $1\,\mu m$. Plasma etching of the thermal oxide could remedy this deviation.

5.2.4 Oxide etch

The standard wet-etching process to structure or remove layers of silicon oxide is to use hydrofluoric acid. Especially in our case, as positive resist is typically used for wet-etch processes. The acid has a high selectivity between silicon and SiO_2 as it does not etch silicon at all. The wet-etch itself is isotropic, which means that if the oxide layer is $1.3\,\mu m$ thick, at least the same amount of SiO_2 is removed laterally, underneath the resist. Therefore, the process needs to be controlled very well, because if the etching lasts too long, the resist gets under etched and the trenches obtain after plasma-etching the substrate will be too wide. The under-etch needs to be considered as a design rule for the reticle design.

Typically it is assumed, that the underetch width is 1.5 times the etched thickness. Therefore, a layer thickness of $2\,\mu m$ and a target trench width of $10\,\mu m$, demands a space

in the mask design of 4 µm. This limits the minimum widths for trenches achievable with wet-etch processes, as the resist needs to be opened at least as much as necessary for the chemical etching processes to work properly. The isotropic character of the process leads to a rounded shape of the sidewalls of the oxide, which is shown in figure 5.4.

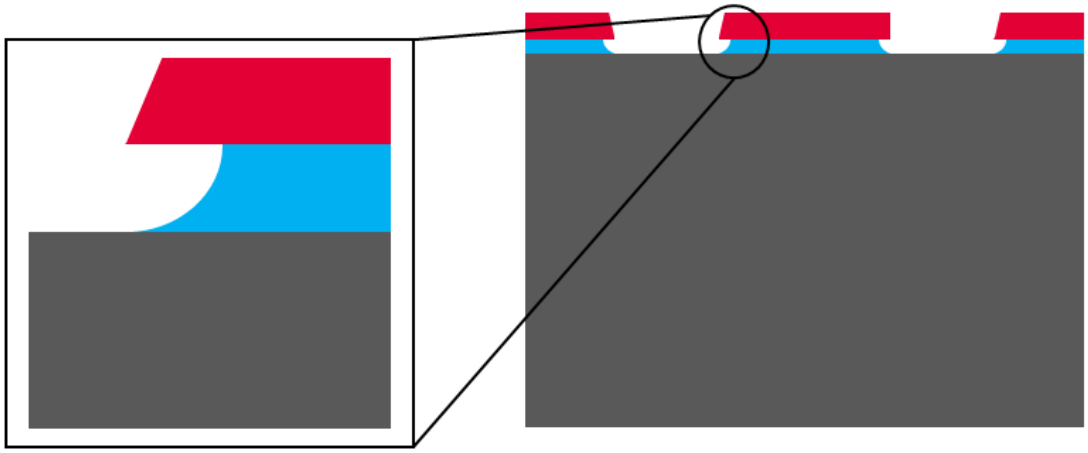


Figure 5.4: Wet-etch of silicon oxide (blue). The structure is given by the photo resist (red). The zoomed picture on the left depicts the rounded shape of the sidewalls of the oxide layer and the underetch. These effects are due to the isotropic character of the etching process and can be controlled by the process duration. The under etch is typically 1.5 times the etched thickness, which is not to scale in the picture.

5.2.5 Deep reactive ion etch (DRIE)

The most challenging fabrication step of YK traps is to etch the trenches into the substrate. This is done by deep reactive ion etching (DRIE) [2], which is an anisotropic plasma-etch process. DRIE allows high aspect ratios of around 50:1. It is a multi-step process in which etching and passivation steps alternate. The scheme of the process is shown in figure 5.5. At first the wafer is covered by a passivation layer (octafluorocyclobutane, C_4F_8), which protects the substrate and prevents etching. Reactive argon ions sputter away the polymer layer from all horizontal surfaces, while the passivation remains on the vertical sidewalls. This is crucial because the subsequent etching step itself is isotropic and would broaden the trenches. After a short etching period using SF_6 (sulfur hexafluoride), there is again a passivation step and the scheme starts from the beginning. This is repeated until the trenches reach their final depth. Due to alternating passivation and etching, the sidewalls of the trenches are not smooth, but have characteristic notches. These notches are called "scallops" and their size is determined by the etching rate. A smaller etching rate reduces their size, but increases the process duration and cost.

[2] Often referred to as *Bosch process* as it was initially developed by employees of Robert Bosch GmbH.

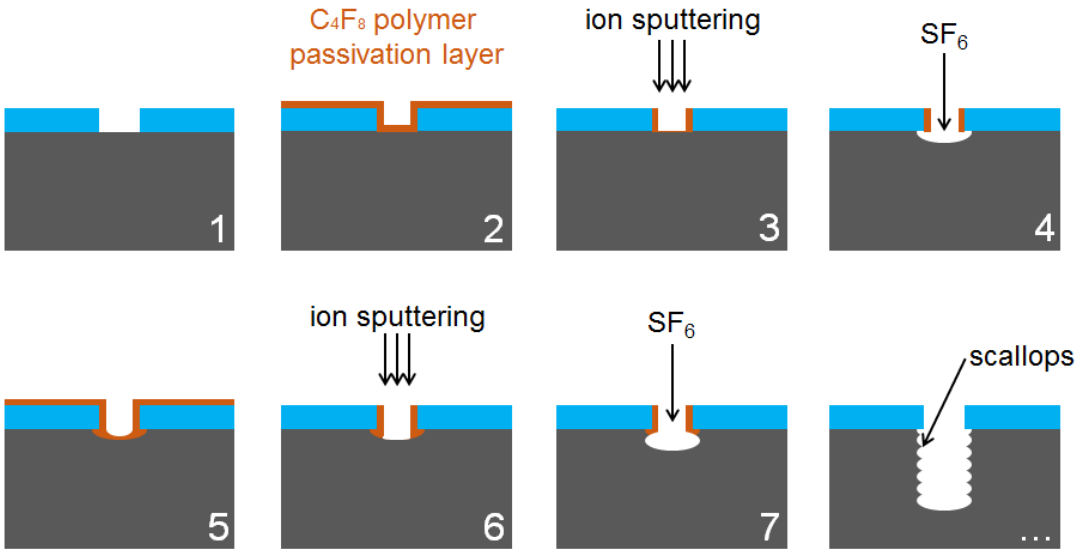


Figure 5.5: Process scheme of deep reactive ion etching (DRIE). The oxide layer (blue) acts as a hardmask for the etching, only the silicon substrate (grey) is etched. The process starts with a passivation step where the wafer is covered by a polymer layer of C_4F_8 (octafluorocyclobutane, orange). This protects the substrate and prevents etching. Reactive argon ions sputter away the polymer layer from all horizontal surfaces, while the passivation remains on the vertical sidewalls. After a short etching period using SF_6 (sulfur hexafluoride), the scheme starts from the beginning with a new passivation step. This is repeated until the trenches reach their final depth. Due to the process the sidewalls of the trenches are not smooth but have characteristic notches called "scallops".

The width of the trenches varies between 5 µm and 15 µm and the target depth is around 100 µm. The trenches need to ensure that the electrodes are well separated. Problems could occur if the evaporation process covers the sidewalls of the trenches with metal. This would lead to short cuts between individual electrodes. For such deep trenches this is very unlikely, but the etching process demands design rules for the resolution that need to be considered. The spacing between two trenches needs to be of a certain width in order make the structures viable. The used reticles contain structures to test the resolution of the etching process. The corresponding structures are pillars and lines with a width of 15 µm, 10 µm, 5 µm, 4 µm and 2 µm as shown in figure 5.6. On the first etched wafers, many of these structures did not withstand the etching process. Initially, barely any of these structures survived and parts of it were torn off the substrate and were found as particles on the wafer. The fallen pillars can be seen in the SEM image of figure 5.6.

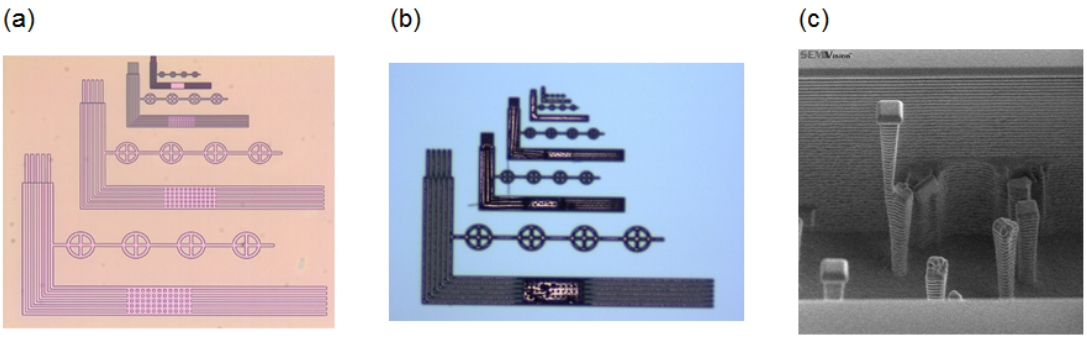


Figure 5.6: Structures to test the resolution of the etching process. The lines and spaces of these structures are 15 µm, 10 µm, 5 µm, 4 µm and 2 µm. **(a)** Micrograph of the structures after Lithography. **(b)** Micrograph of the structures after DRIE. The structures did not survive the process. Due to the surface height variations (topology), the structure can not be focused very well. **(c)** Scanning electron micrograph of fallen pillars with 10 µm width. This picture was taken after the follow-up process oxide deposition.

In order to optimize the process, the target depth was reduced to around 70 µm. As a result, the resolution got much better and the amount of particles on the wafers was strongly reduced. Figure 5.7 depicts SEM images of the trenches of a YK trap and surviving pillars. The scallops have a radius of roughly 1 µm and the trenches are around 70 µm deep.

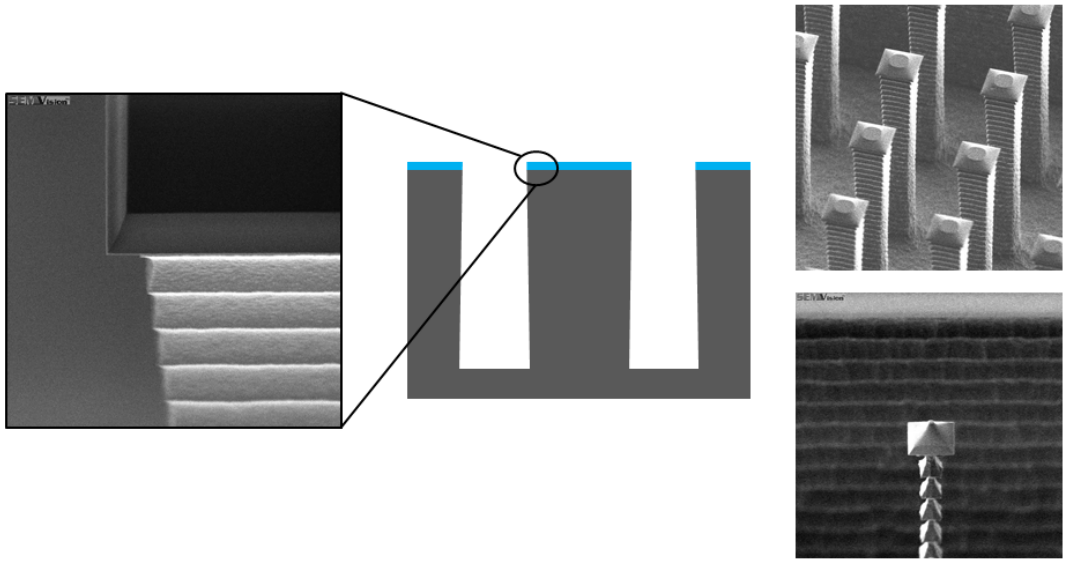


Figure 5.7: SEM images after optimization of the DRIE. **Left:** SEM image of the trenches of a YK trap and schematic cross section that shows the substrate (grey) and the thermal oxide layer (dark blue). The oxide layer is rounded due to the isotropic wet-etch. The sidewall of the trenches show the characteristic scallops with a radius of roughly 1 µm. The trenches are around 70 µm deep. **Top right:** SEM image of surviving pillars with 10 µm width. The pillar's hat is the thermal oxide layer which is rounded due to the isotropic wet-etch. **Bottom right:** The process is now optimized to a level that even the 5 µm pillars survive. The hardmask is sharply pointed and the scallops leave just enough substrate left to prevent the pillar from collapsing.

At this point it is important to note that the scanning electron microscope that can be used inside the cleanroom allows only rough estimations of the depth of the DRIE (±10%). The actual geometry of the trenches cannot be checked. This can only be determined by analysing the wafer's cross section. For this purpose, one wafer is cut in half after the follow-up process oxide deposition. This cross section analysis allows us to measure the geometry of the trenches and the thickness of the individual layers. These results are presented in section 5.3.

5.2.6 Oxide deposition

The easiest way to cover the surface of the wafer and the sidewalls of the trenches with a uniform oxide layer would be to grow the layer thermally. As mentioned before, this is forbidden after DRIE in the clean room of Infineon Technologies at Villach. The alternative way is to deposit oxide. The chosen process deposits 2.5 µm of undoped silicate glass (USG) via plasma enhanced chemical vapour deposition (PE-CVD) with tetraethylorthosilicat (TEOS) as precursor gas. As a rule of thumb, about one-third of the deposited layer thickness is deposited on the vertical sidewalls of the trenches. A SEM image of the sidewall of a trench is given in figure 5.8. The scallops and the hardmask are covered by the deposited oxide.

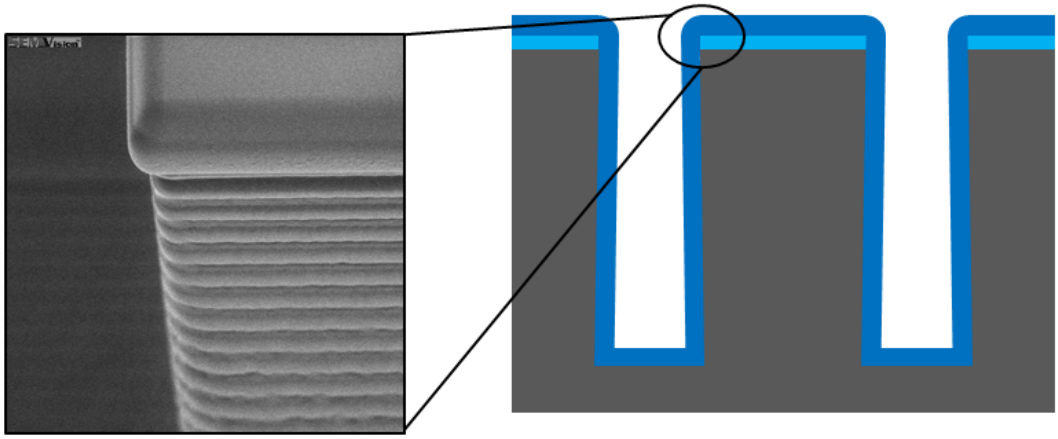


Figure 5.8: SEM image of a trench after oxide deposition. The scallops and the hardmask are covered by the oxide. The top surface of the silicon substrate (grey) is now covered by a thermal oxide layer (light blue) and a deposited one (dark blue).

5.2.7 Metallization

The final layer of the YK traps is the metal stack that forms the electrodes. Michael Niedermayr used a metal stack of 2 nm titanium and 500 nm gold. A comparable and available process at Infineon Technologies in Villach is to deposit 50 nm titanium, 100 nm platinum and 600 nm gold by means of evaporation. In this combination, the titanium acts as a adhesion promoter and the platinum prevents diffusion and formation of intermetallics between titanium and gold. One of the wafers after metallization is shown in figure 5.9.

The wafer is already prepared for our last process, namely dicing. For this reason the wafer sticks to a foil in a dicing frame.

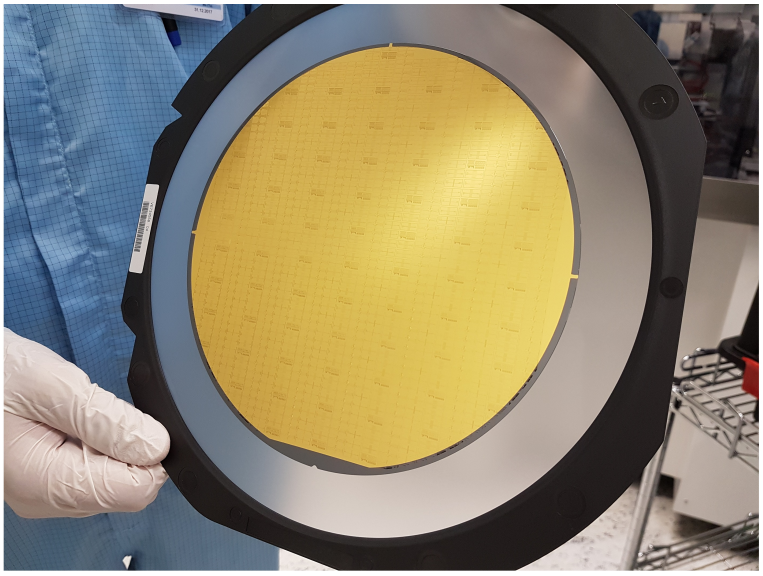


Figure 5.9: One of the wafers after metallization. The wafer is already prepared for dicing as it sticks to a foil in a dicing frame.

5.2.8 Dicing

The final step of the fabrication is dicing the wafers into single chips. There exist various processes which can be chosen according to the properties of the wafers and chip sizes, like for example laser dicing for thin wafers, stealth dicing or mechanical dicing [85, 86]. In our case dicing is very challenging, because the metal stack is not removed at the scribelines. This is considered as a serious violation of the design rules for dicing and forces the use of mechanical dicing.

The problem with metal in the scribeline is the following: The blade is composed primarily of grit and bond. The grit is a hard material like diamond which actually performs the processing. The bond acts like a substrate and holds the grit like raisins in a bread. During the dicing process, the blade performs a self-sharpening effect, as the bond wears out. This causes the used grit to fall off and new grit comes to the blades surface. This effect is harmed by materials that stick to the blade, which is called loading. If the loading gets too strong, the blade does not cut any more but rubs until it finally breaks. For this reason there exist design rules for the scribe lines which include the width of the scribelines and the allowed layer stack.

As there is no way to remove the metal without an additional reticle, the mechanical dicing process had to be adapted. Several blades broke during the first tries and the cooling water distributed many particles all over the wafer. Different types of blades with different grit sizes where used. The surface tension of the cooling water is weakened via additives in order to prevent particle adhesion. Example micrographs of the scribelines are shown in figure 5.10. At the vertices of the horizontal and vertical scribelines the metal tends to peel off a bit. This is due to the high mechanical stress at these points. Even though we

reduced the amount of particles at the wafers by using additives [3] for the cooling water, we still find some fallen pillars washed away and distributed all over the wafer.

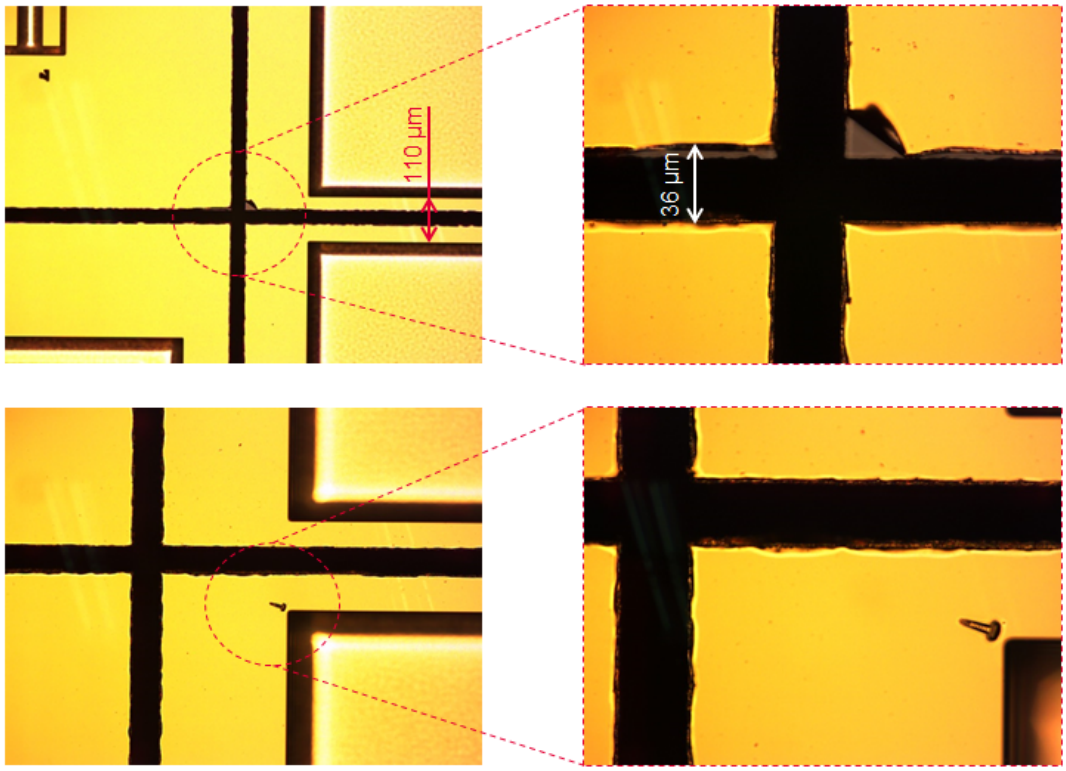


Figure 5.10: Micrographs of the scribelines after-dicing. **Top row:** The scribelines are around 36 µm wide. The smallest distance between structures is 110 µm. At the vertices of the scribelines the gold tends to peels off a bit. **Bottom row:** Fallen pillar displaced by the cooling water.

As mentioned above, the wafer is glued to a foil for sawing. The saw cuts through the wafer, while the foil is sawn only partially. Subsequently, the foil is exposed to UV light to weaken the adhesive. In this state, it is possible to transport the wafer and individual chips can be removed with tweezers.
Eight diced wafers were delivered to Innsbruck: Seven of them with the target substrate (float-zone, high resistivity) and one dummy wafer using standard silicon substrate. Each wafer contains 63 reticle shots where every shot contains 12 chips. This gives a total of around 5300 chips for the seven wafers. The purpose of the dummy wafer was to test whether there were residues of the additives of the cooling water on the wafers surface.

5.3 Failure analysis

In order to test whether the fabricated traps are functional, we gave some samples to the failure analysis department. The failure analysis of Infineon Technologies in Villach provides many interesting tools and processes to analyse wafers or single chips. This includes different electric tests with DC and RF voltages, Auger analyses, energy dispersive

[3] DISCO, StayClean-F

X-ray spectroscopy (EDX), focused ion beam microscopy (FIB) and scanning electron microscopy of cross sections.

5.3.1 Cross section and layer analysis

The first step of failure analysis is to determine the shape of the trenches and thickness of the oxide layers. At that time when we gave the wafer to the failure analysis, the colleagues in Villach were very busy and decided to sent our wafer to another Infineon Technologies site, namely Kulim in Malaysia. The outcome of this analysis is shown in figure 5.11. The analysed trench has a width of 6 µm and a depth of 67 µm.

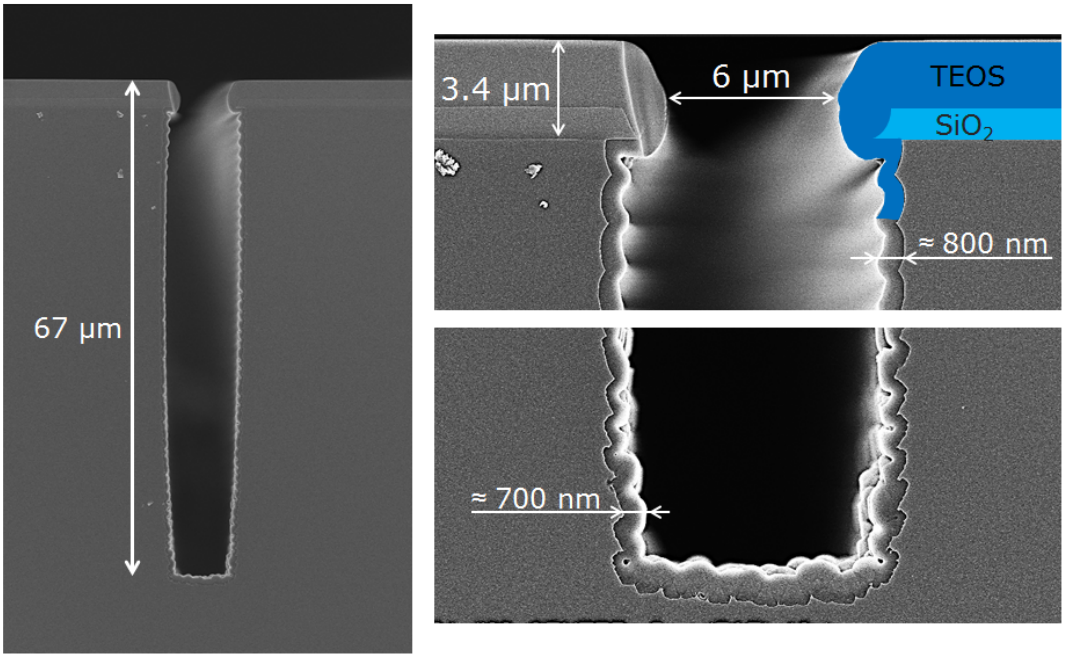


Figure 5.11: SEM images of the cross section analysis. The analysed trench has a width of 6 µm and a depth of 67 µm. The oxide layer on top has a thickness of 3.4 µm, resulting from a residual thickness of the hardmask of 1 µm plus 2.4 µm deposited oxide. The sidewalls are covered with roughly 800 nm (700 nm) oxide at the top (bottom) of the trench. The analysed wafer has no metal on top.

The sidewalls are covered by the deposited oxide. The deposited oxide has a thickness 2.4 µm on the top surface, 800 nm (700 nm) at the top (bottom) of the sidewalls of the trench. The hardmask still has its rounded shape, even after it got thinned by the DRIE and its residual thickness is 1 µm. This adds up to 3.4 µm of oxide at the wafers surface. The trenches with a width of 11 µm are $\simeq 4$ µm deeper compared to 6 µm wide trenches. None of the trenches has an undercut at the sidewalls, but it is assumed that the depth is sufficient to separate the electrodes. To be sure that there is no electrical contact between the electrodes we performed electrical tests.

5.3.2 Electrical tests

The electrical testing of the traps makes up the second part of the failure analysis. On the one hand this checks whether the electrodes are well separated by the trenches. On the other hand, the DC break-down voltage is measured in order to make sure that the traps withstand the necessary voltages for ion trapping experiments. Unfortunately, it is not possible to check the RF behaviour of the traps because the RF measurements can only be made at room temperature. As the behaviour of silicon is quite different at $T = 4\,\mathrm{K}$ compared to room-temperature, this measurement would not provide any meaningful data. A micrograph of a tested sample is shown in figure 5.12.

For the measurement, the sample is placed on a grounded metal plate and contacted via needles to apply DC and ground (GND) potential. The setup allows us to ramp up the DC voltage while measuring the current. Additionally, it is possible to observe the sample through an optical microscope. Two traps with 5 µm and 15 µm trench widths are tested and their breakdown voltage is found to be around 350 V and 425 V, respectively. The test is done at atmospheric pressure and even though trapping experiments are in UHV conditions the tests are suitable to learn about the actual behaviour of the trap [87, 88]. The purpose of these tests is to figure out whether the traps can withstand the voltages necessary for ion trapping experiments. Implementation of a trap that would end in an electrical failure needs to be avoided.

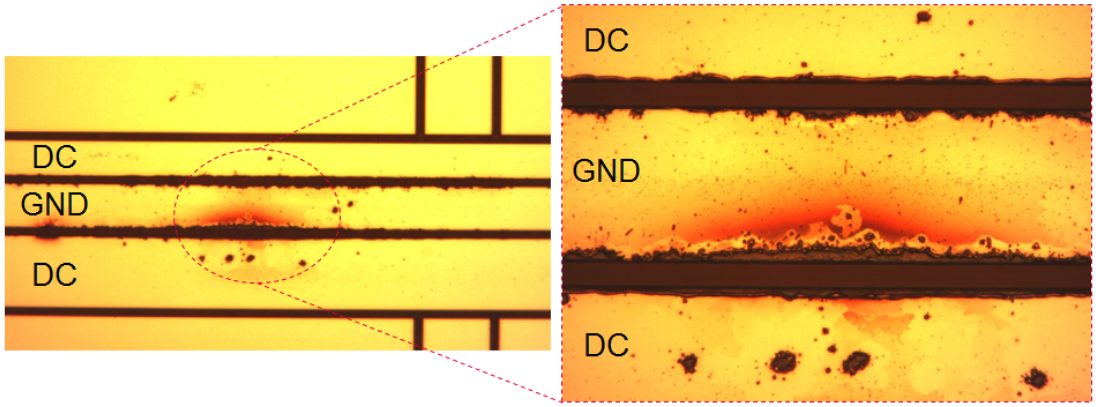


Figure 5.12: Micrograph of a tested sample with 5 µm trench widths. The breakdown voltage is around 350 V, at which field electron emission caused by Fowler–Nordheim tunnelling sets in [89].

The effect behind the breakdown is field electron emission caused by Fowler–Nordheim tunnelling [89]. There is no visible damage of the silicon oxide and substrate.

5.4 Workflow for the fabrication of 2D linear trap arrays

The second trap design that is part of this work is that of the 2D trap arrays. The corresponding mask design is based on the demonstrated simulations of Chapter 4. The implemented workflow is briefly summarized in subsection 5.4.1, including a more detailed

description of the via-etching process. The chosen processes and layer thicknesses lead to design rules, which are discussed in subsection 5.4.2.

5.4.1 Three metal layers with vias

The fabrication of the 2D linear trap array is based on the use of three structured metal layers with vias. Similar to the fabrication of the YK traps, the workflow starts with a thermal oxidation. The target thickness is again 1.3 µm in order to electrically isolate the substrate. The first metal layer has a thickness of 750 nm aluminium-silicon-copper (AlSiCu) with 25 nm of titanium nitride (TiN) on top. The TiN has two purposes: It promotes the adhesion between deposited oxide and AlSiCu and acts as an anti-reflective coating necessary to do lithography on the deposited oxide layer. The thicknesses of the second and third metal layer are 1000/25 nm AlSiCu/TiN and 2000 nm AlSiCu, respectively. The AlSiCu has 98.5% aluminium, 1% silicon and 0.5% copper and the layers are applied by sputtering. The first two metal layers are structured by means of plasma etching, whereas the third metal layer is wet-etched. The wet-etch for the third metal layer is due to its thickness. It is feasible to test a plasma-etch process for this layer too in order to reduce the widths of the trenches that separate the electrodes. Between the metal layers we deposit 2200 nm undoped silicate glass (USG) which isolates the metal layers from each other. These oxide layers are structured in order to form vias.

The process to etch the vias has two stages: It starts with a short isotropic etch, followed by an anisotropic part. This combination allows us to etch vias where the minimum dimension is given by the thickness of the corresponding oxide layer. In our case the vias have a dimension of 15 μm $\times$ 15 µm which is bigger than necessary. This allows us, if necessary, to fabricate traps with thicker oxide layers between the metal layers without the need of new reticles. The process sequence for the formation of vias is schematically shown in figure 5.13. At this point, the wafer already has its thermal oxide layer, first metal layer and first deposited oxide layer. For simplification the schematic includes an unstructured first metal layer.

After a lithography step, the via etching starts with an isotropic stage. This initially opens the oxide layer which benefits the further etching process. The anisotropic part is a plasma etch process, where the sidewalls are covered by a polymer layer which reduces the lateral etching rate. The final shape of the via is similar to a glass of wine, where the lateral extension of the etched oxide rim is influenced by the thickness of the oxide layer. The opening of the via at its bottom needs to be around three to four times the thickness of the oxide layer. In the presented case this would be 6.6 $-$ 8.8 µm. The actual design includes vias with 15 µm width, which would allow us to fabricate the traps with a thicker oxide layer without the need of a new mask. For thicker oxide layers one needs to adapt the process duration of the anisotropic etching part. Once the via etch is finished, the TiN layer is removed by a cleaning process and the resist is stripped, followed by the sputter process for the second metal layer. The use of a sputter process instead of an evaporation process is necessary, as it allows a thicker metal deposition and a good coverage of the sidewalls. This is crucial to ensure an electric connection between the metal layers.

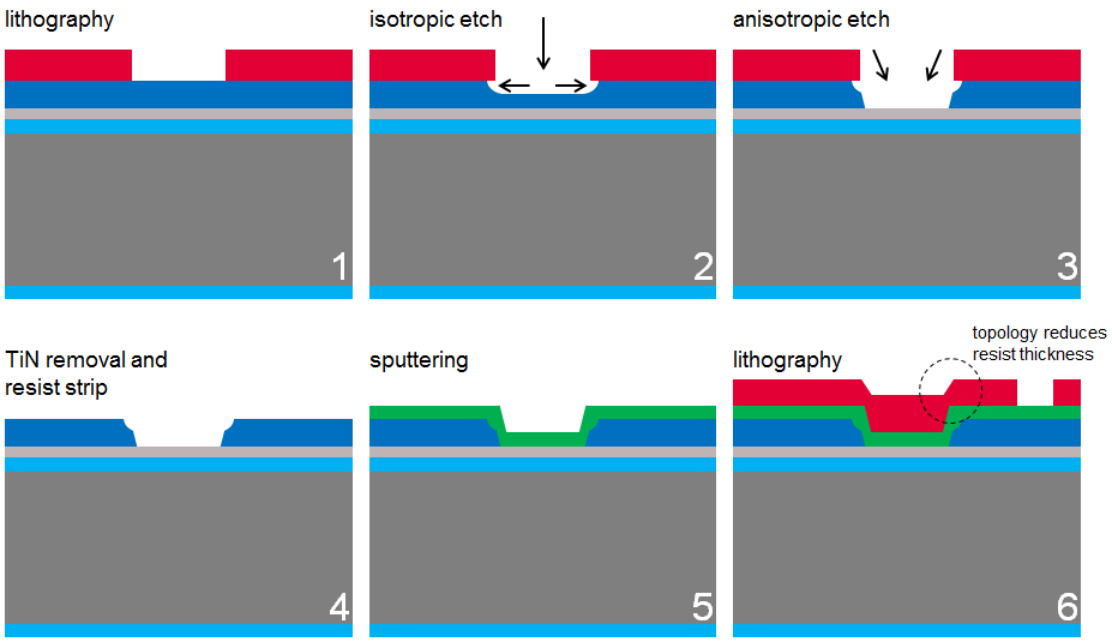


Figure 5.13: Process sequence to form vias between the first two metal layers. The substrate (dark grey) is initially covered with a thermal oxide layer (light blue), the first metal layer (light grey), the deposited oxide layer (dark blue) and the photo resist (red). The etching process has an isotropic and an anisotropic part to etch space-saving vias. After the removal of the TiN layer inside the vias and the resist strip, the second metal layer (green) is deposited by a sputter process. The follow-up lithography allows us to structure the second metal layer. Due to the surface height variations (topology), the resist layer gets very thin at the edges of the vias. This can be a problem if the resist consumption during the metal etch is of such a strength, that the residual thickness at these edges is not sufficient to protect the edges from the plasma.

The next step is lithography to structure the second metal layer. Due to the surface height variation it is important to use quite thick resist layers. In the actual case, 3.9 µm of positive resist. Especially at the edges of the vias the resist layer gets very thin, which can be a problem, if the resist consumption during the metal etch is of such a strength, that the residual thickness at these edges is not sufficient to protect the edges from the plasma. This needs to be considered before lithography and checked after the etching process.

The vias between *metal 2* and *metal 3* layers are fabricated in the same way. Vias that connect *metal 1* and *metal 3* are two vias, each feeding through one oxide layer, which are designed to be concentric (via-in-via). This reduces the lateral extension but increases the topology at the top surface, compared to two vias which are close by and each connect two metal layers independently. As the thicknesses for the three metal layers and their corresponding etching processes are different, this brings individual design rules for the single reticles. As mentioned before, the first two metal layers are structured by means of plasma etching, whereas the third metal layer is wet-etched. The limitations are shortly summarized in the following.

5.4.2 Design rules and limitations

In order to ensure that the designed traps can be produced, there exist rules and limitations for the reticle design. These design rules are given by the chosen processes and rely on the experience of the single-process experts at Infineon Technologies. The rules determine the smallest electrode and gap size for every layer. These dimensions are influenced by the corresponding layer thickness and the etching processes. For example: Typically, the minimum gap size for a wet-etch process is bigger than for a comparable plasma-etch process, because plasma etching processes are more directed. The corresponding dimensions for the individual metal layers are summarised in table 5.1.

Layer	AlSiCu/TiN	Etch process	Smallest electrode size	Smallest gap size
metal 1	750/25 nm	plasma	2 µm	5 µm
metal 2	1000/25 nm	plasma	2.8 µm	5 µm
metal 3	1000/0 nm	wet	14 µm	9 µm

Table 5.1: Design rules for the three metal layers. The smallest electrode and gap sizes are mainly influenced by the corresponding layer thickness and the etch process used to structure the layer. In the case of *metal 1* and *2*, the deposition of the intermediate oxide also plays a role for the gaps dimensions.

There is a clear difference in the resolution for the chosen wet- and plasma-etch processes. The minimum gap size for *metal 1* and *2* is mainly limited by the deposition process for the oxide layers. The 2200 nm of oxide fill up the gaps and cover all the lines. The minimum width of the spaces ensures that the gaps are filled by the oxide before they are closed. The oxide acts as a dielectric between the lines and air pockets can lead to electric failures. How the trenches are filled by the deposition is schematically shown in figure 5.14.

Figure 5.14: Deposition of 2200 nm of oxide to fill the gaps. The first deposited oxide layer (dark blue) and the structured second metal layer (green) are covered by the second deposited oxide layer (pink). During deposition, the oxide fills and closes the gap. The minimum gap size ensures that the gaps are filled properly without the formation of air pockets.

The workflow used for the 2D linear trap arrays has the advantage that all the chosen processes are used for other products at Infineon Technologies in Villach as well. Therefore, a lot of know-how from the individual experts is available.

Another important aspect of our fabrication workflow is that it uses exclusively processes from the "front-end-of-line" [4] (FEOL). This allows effectively a wider range of tools

[4]The front-end-of-line (FEOL) covers all processes before deposition of metal. Tools and wafers from

available for the fabrication, without the restrictions that the use of back-end-of-line (BEOL) processes would entail for subsequent fabrication steps. This is because the use of back-end-of-line tools may cause contamination with critical materials such a gold or platinum, which forbids the later use of FEOL processes. Also, complying with the design rules for the width and the layer stack of the scribelines strongly simplifies the dicing process compared to the Yedikule traps.

After the fabrication of Yedikule traps the diced wafers are delivered to Innsbruck. The wafers still stick to the foil necessary for dicing and the single chips can be picked off with tweecers. At the university's clean room the chips are optically inspected and the wire bonding is performed. In this form the traps are ready for the experiments. The experimental characterization takes place in the "Cryolab". In the following chapter some important parts of the experimental setup are described. A more detailed version can be found in Michael Niedermayr's PhD thesis [23].

FEOL and BEOL must not be mixed in order to avoid cross-contamination of FEOL wafers by metal. Most tools are FEOL classified since the majority of process steps in a semiconductor fab is carried out before metal deposition.

Chapter 6

Experimental setup

The ion trapping experiments presented in this thesis were carried out in a cryogenic environment. The setup was mainly built by two former PhD students, Michael Niedermayr and Muir Kumph. All the details regarding the setup are given in their PhD theses [23, 90]. This chapter starts with a short motivation why to operate ion traps in a cryogenic environment in section 6.1, followed by a brief description of the cryostat and the vacuum chamber in section 6.2. Finally, the optical setup is briefly presented in section 6.3. During the time of my master's thesis, the lab was mainly operated by two current PhD students, Kirill Lakhmanskiy and Philip Holz. While Philip supervised my simulations, Kirill prepared the traps for the experiments and did most of the measurements.

6.1 Cryogenic environment

The use of trapped ions for quantum information processing requires that the traps are operated in ultra high vacuum (UHV). UHV refers to a preassure of $10^{-11} - 10^{-12}$ mbar which prevents the ions from collisions with background gases and therefore reduces the risk of an ion loss. Such low pressures are in some respect easier to achieve for vacuum chambers at cryogenic temperatures because of the cryopumping effect [91]. First, a turbomolecular pump evacuates the system to a medium vacuum of around 10^{-6} mbar. As second step, the cryostat is turned on and at $T \approx 10\,\mathrm{K}$ most residual gases have a stationary pressure of $< 10^{-12}$ mbar and stick to the cold surfaces due to absorption [91]. The reachable pressure of $< 10^{-12}$ mbar refers to extreme high vacuum (XHV).
The two steps typically take one or two days which reduces the timespan to change from one ion trap to another (turnaround time). Such an exchange includes heating the system to room temperature, breaking the vacuum, changing the trap, pumping to a medium vacuum and cooling down again. This is a very short time compared to room temperature setups, which require typically at least one week of baking time to achieve such a high vacuum. A low turnaround time is necessary for short development cycles in order to test different trap designs and fabrication parameters rather quickly. Furthermore, the low temperatures suppress the outgassing of the materials and allow therefore the use of some plastics and adhesives.

Besides significant lower turnaround times cryogenic setups also help to reduce the motional heating rate. This was investigated by several independent experiments [48, 92–94]. The listed experiments were very different from each other and many details of the experiments cannot be directly compared. Therefore they also vary in their quantitative observation of how the heating rate depends on the operation temperature. Nevertheless, all the results clearly show that the heating rate decreases for lower trap temperatures. Starting from acceptable or even high heating rates at room temperature the experiments report a reduction of two to seven orders of magnitude, respectively, while cooling from 300 K to < 10 K. The reduced heating rate at low temperatures can be attributed to different effects. Typical cryogenic setups provide black-body shields to protect the ion and the trap. As they are made of materials like copper or aluminium, their conductivity increases for lower temperatures which makes them more efficient and the noise due to EMR is suppressed [60, 95]. Typically surface noise is strongly reduced at low temperature which is responsible for the lower heating rate at low temperature compared to setups at room temperature.

Although the advantages mentioned speak strongly for using a cryostat this also brings some disadvantages. First to mention here are the higher costs compared to traditional room-temperature setups. Depending on the cooling system used cryostats can be very complex and therefore expensive. The coolant, in most cases liquid helium, increases the operation costs. The experimental setup of the Innsbruck Cryolab includes a Gifford-McMahon cryostat (closed-cycle cryostat) to provide a cryogenic environment for the experiments (see section 6.2).
Another disadvantage is given by the mechanical vibration due to the cooling process. For closed-cycle setups the corresponding amplitudes reach values of roughly 10 µm [96]. This can cause a relative movement of the laser beam with respect to the ion which harms the experiments [32]. Therefore, a vibration-insulation system is installed and reduce vibrations well below 1 µm (~ 200 nm in the Cryolab setup).
A third disadvantage comes with the thermal expansion. The individual materials behave different during the cooling process which might cause thermal stresses between the layers of the trap. This can lead for example to cracks or breakage of wire bonds.

6.2 Cryostat and vacuum chamber

The used cryostat is a closed-cycle Gifford-McMahon system with two stages and the operation mode is very similar to an inverted Stirling cycle [97]. The working principle is based on four steps which are periodically repeated:

(1) With the system at high pressure, the displacer pushes liquid helium from the hotter stage towards the cooler stage. The liquid flows through the regenerator and gets precooled, as the regenerator stores its heat.

(2) The valves are used to drop the pressure in the system. The necessary energy for an isothermal expansion of the helium is taken from the cooler stage.

(3) After this cooling procedure, the displacer pushes back the helium towards the hooter

stage. The stored heat from the regenerator is used to heat up the liquid while it floats back.

(4) As final step, the pressure is increased again. During an isothermal compression the thermal energy of the liquid is used to heat up the hotter stage.

A schematic of the used cryostat is shown in figure 6.1. Here, the displacer and the regenerator are combined. Their movement is steered by a motor. The two reservoirs are provided by a compressor and the pressure of the system can be controlled by two valves, one for low and high pressure, respectively. The first stage can reach a temperature of $< 50\,\mathrm{K}$ and is called the 50 K stage. The second stage could reach a temperature of $< 4\,\mathrm{K}$, but due to additional heating while operating the trap it reaches only $< 10\,\mathrm{K}$. Therefore it is called the 10 K stage.

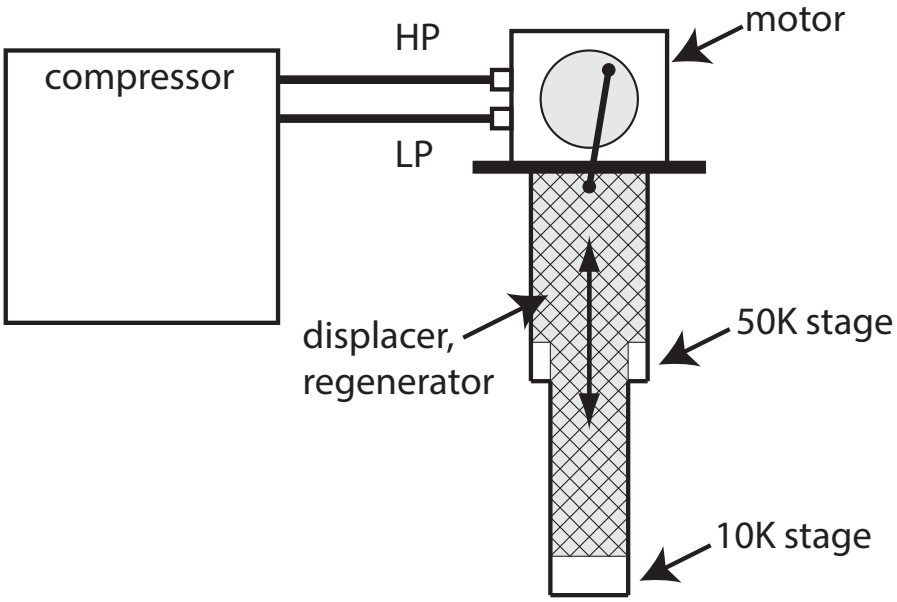


Figure 6.1: Schematic of the used Griford-McMohan system. The two stages have a temperature of $< 50\,\mathrm{K}$ and $< 10\,\mathrm{K}$. The displacer is combined with the regenerator and both are moved by a motor. High and low pressure lines (HP, LP) are provided by a compressor and their connections are controlled by valves. Figure taken from [23].

To reduce these vibrations, a GMX-20 [1] adapter is connected to the cryostat by a rubber bellow. The closed volume between the adapter and the cold stage is filled with helium. This reduces the amplitude of the vibrations to around $200 - 300\,\mathrm{nm}$ [23]. The GMX-20 adapter, together with a CF160 full nipple, forms the actual vacuum chamber and the whole setup is mounted on an optical table. A schematic cross section of the chamber is shown in figure 6.2. The ion trap itself is mounted at the bottom of the chamber, which region we call the octagon and the trap mount ensures a good thermal conductivity to the 10 K stage. Additionally, the trap is surrounded by a 50 K and 10 K chopper shield. These shields are thermally connected to the corresponding stages of the cryostat and protect the trap from thermal radiation. The valve allows us to connect the vacuum pump station to the chamber and electrical connections are integrated by feedthroughs (BNC and D-sub). The actual chamber offers twenty connections, including two independent RF

[1] Advanced Research Systems, GMX-20

lines, two lines to measure the actual RF voltage at the electrode and sixteen DC lines. These connections are all anchored to the cold stages in order to reduce the amount of thermal energy brought to the trap.

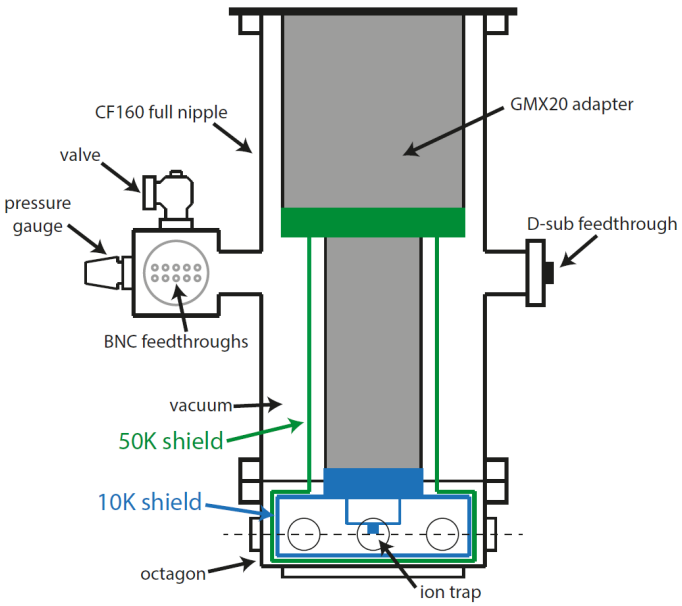


Figure 6.2: Schematic cross section of the vacuum-chamber. The vacuum chamber mainly consists of a GMX-20 adapter together with a CF160 full nipple. The ion trap itself is mounted at the bottom of the chamber inside the octagon. It is shielded by a 50 K and 10 K copper shields which are connected to the corresponding stages of the cryostat (green and blue). The valve allows us to connect the vacuum pump station and the feedthroughs provide electrical connections (BNC and D-sub). Figure taken from [23].

The octagon gets its name from the eight viewports that provide optical access to the trap. The opened octagon with a mounted Infineon trap inside is shown in figure 6.3. The trap mount is made of copper and includes a temperature sensor. The wire bonds connect the DC electrodes to the DC filters and the RF electrodes to the matching network. This network consists of a variable capacitor and a small homebuilt copper coil. It is used to match the impedance of the RF circuit to that of the function generator (50 Ω). This matching reduces reflections of the RF signal. The holes in the shields are the viewports which are used to shine in the required lasers. The calcium oven assembly is also attached to a CF40 viewport flange.

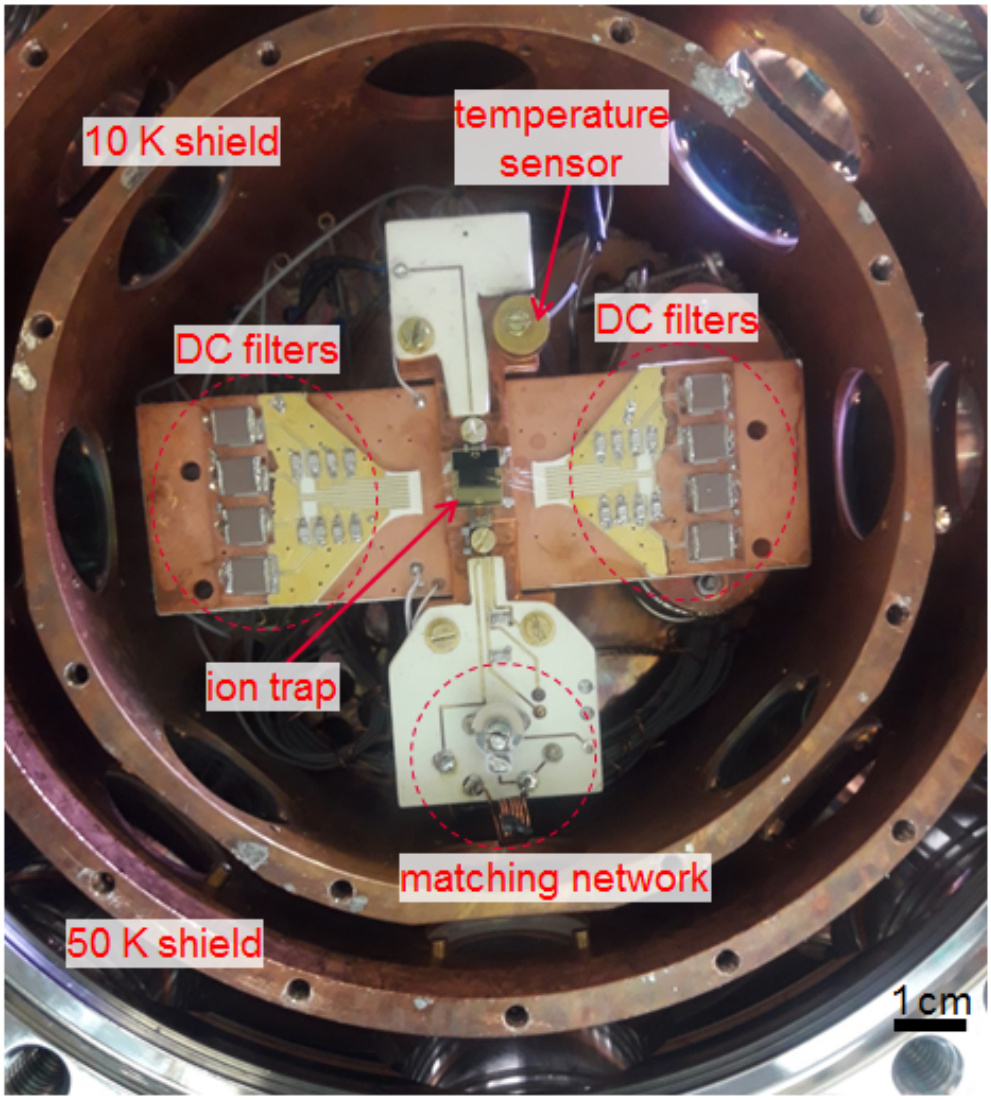


Figure 6.3: View of the open octagon. The ion trap is mounted in the center and the mount includes a temperature sensor. Wire bonds connect the DC electrodes of the chip with the DC filters and the RF electrodes with the matching network. This network consists of a variable capacitor and a small homebuilt copper coil. The 50 K and 10 K shields surround the trap and provide the necessary optical access via eight viewports. Figure courtesy of Kirill Lakhmanskiy.

The oven generates a beam of neutral calcium atoms which is directed towards the trapping region. Two pairs of magnetic coils are attached to four of the octagon viewports and provide a homogeneous magnetic field across the trapping region. This magnetic field is used to split the Zeeman sublevels in order to resolve the transitions of the trapped ion (see section 2.4). The optical setup is briefly described in the following, all the details can be found elsewhere [90, 98, 99].

6.3 Optical setup

The vacuum chamber is mounted on an optical table, such that the necessary lasers can shine through the viewports of the octagon. The optical setup includes six different wavelengths: 422 nm and 375 nm for ionization of the calcium atoms, 397 nm and 866 nm for Doppler cooling and state detection and 729 nm and 854 nm are used in relation to the qubit transition (see section 2.2 and 2.4).

The laser beams configuration with respect to the vacuum chamber and the used coordinate system are depicted in figure 6.4. The 422 nm, 375 nm, 397 nm, 866 nm and 854 nm beams are overlapped by dichroic filters [2] (SR). These beams share one lens (main lens) before entering the chamber via viewport (1). The 397nm and the 729nm beams enter the chamber via viewport (5) and (3), respectively. The calcium oven is attached to viewport (2). The 422 nm and 397 nm beams are generated by a sequence of frequency doubling [90, 98] while the 729 nm light is provided by a titanium-sapphire laser and amplified by a tapered amplifier [99]. The other wavelengths originate directly from laser diodes [90, 98]. The particular purpose of the individual wavelengths during the experiments is stated in figure 2.3 and discussed in section 7.1.

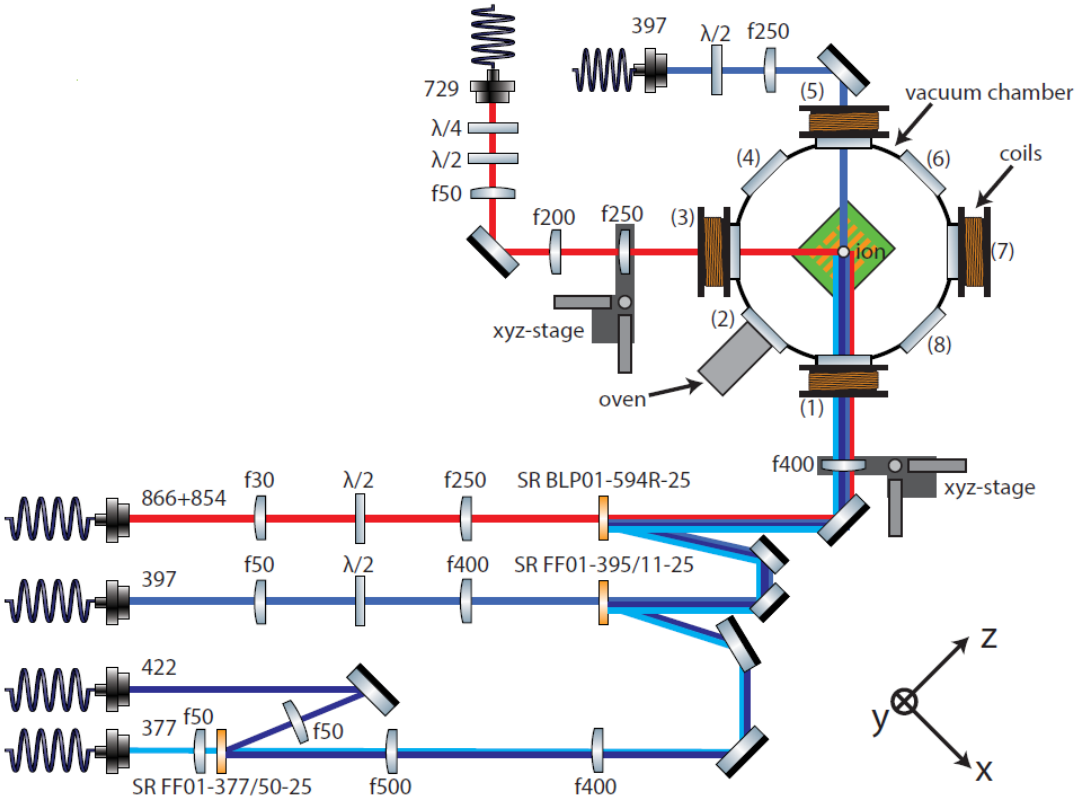


Figure 6.4: Schematic of the configuration of the lasers with respect to the vacuum chamber. The coordinate system is consistent with the one chosen for the trap. Dichroic filters (SR) are used to overlap the 422 nm, 375 nm, 397 nm, 866 nm and 854 nm beams. These beams share one lens and enter the chamber via viewport (1). The 397 nm and the 729 nm beams are directed such that they enter the chamber via viewports (5) and (3), respectively. The calcium oven is attached to viewport (2). Figure taken from [23].

[2] Semrock, 2x SEM-FF01-395/11-25, 1x SEM-FF01-417/60-25

The alignment of the lasers at the position of the ion trap is such that the laser beams cross each other under a certain angle. Depending on the trapping height, the lasers are relatively close to the trap surface. During realignment of the laser beams it is important to avoid collisions of the beams with the trap. The lasers provide enough energy for the electrons in the substrate to overcome the band gap of silicon and create electron-hole pairs. This is briefly discussed in subsection 7.2.1.

Chapter 7

Experimental results

The presented experiments are all carried out with YK traps fabricated by Infineon Technologies in Villach, as described in section 5.2. The first part of this chapter describes the basic procedure to trap an ion. After the first successful trapping attempts, the trap needs to be characterized by heating rate measurements. The follow-up part is about these measurements which where mainly carried out by Kirill Lakhmanskiy. The results are briefly discussed and compared with those from Michael Niedermayr's experiments. The details on the measurements will be given in Kirill's PhD thesis. In relation with these measurements, the problems concerning stray light are addressed. The final part of the chapter provides ideas on how to improve future surface ion traps. These proposals include things that could be realised during follow-up projects together with Infineon Technologies.

7.1 Procedure to trap an ion

First, the delivered wafers are brought to the university's cleanroom. During the shipment the diced wafers still stick to the foil which was used for dicing. After dicing, the foil is exposed to UV light so that the single chips can be picked off with tweecers. The final preparation of the traps in the university's cleanroom include an optical inspection and wire bonding. The wirebonds are made of gold, have a diameter of 25 µm and connect the trap electrodes with four printed circuit boards (PCBs) (fig. 6.3). The DC electrodes are connected with RC filters and RF electrodes are connected to the resonator from one side and capacitive voltage divider (cap. divider) from another side. The cap. divider is installed next to the trap and enables a measurement of the RF voltage at the trap [23]. Some of the DC electrodes are connected twice, allowing an independent measure of the voltage applied to a trap DC electrode. Thus, broken wires can be detected in situ. The trap with the attached wire bonds is depicted in figure 7.1. Due to a failure in the mask design, the wire for the central DC electrode on the right side could not be bonded at the bonding pad. This electrode needs to be bonded somewhere closer to the RF electrodes. The RF voltage is provided by a function generator. An RLC resonator is used to amplify the signal in order to allow low RF input power ($< 100\,\mathrm{mW}$) [23]. The remaining surface of the chip is grounded by an additional bond wire.

After bonding, the trap is mounted to a copper carrier which is connected to the 10 K stage of the cryostat. The trap cannot be glued to the carrier as copper and silicon contract differently when cooled. This would cause tensions and the trap would lose the connection to the carrier and the thermal connection would get insufficient. As an alternative, the trap is fixed by titanium clamps which are bolted down to the copper carrier by brass screws. The clamps provide a reliable mounting that can withstand several cooling cycles. Before clamping, the backside of the trap is coated with a thin layer of a heat-conducting grease which improves the thermal conductivity between the trap and the carrier. The trap has an additional connection for an in situ measurement of the resistivity of the substrate. Furthermore this connection provides the possibility to apply a DC bias to the substrate. This should allow us to investigate the generation of charge carriers in the substrate.

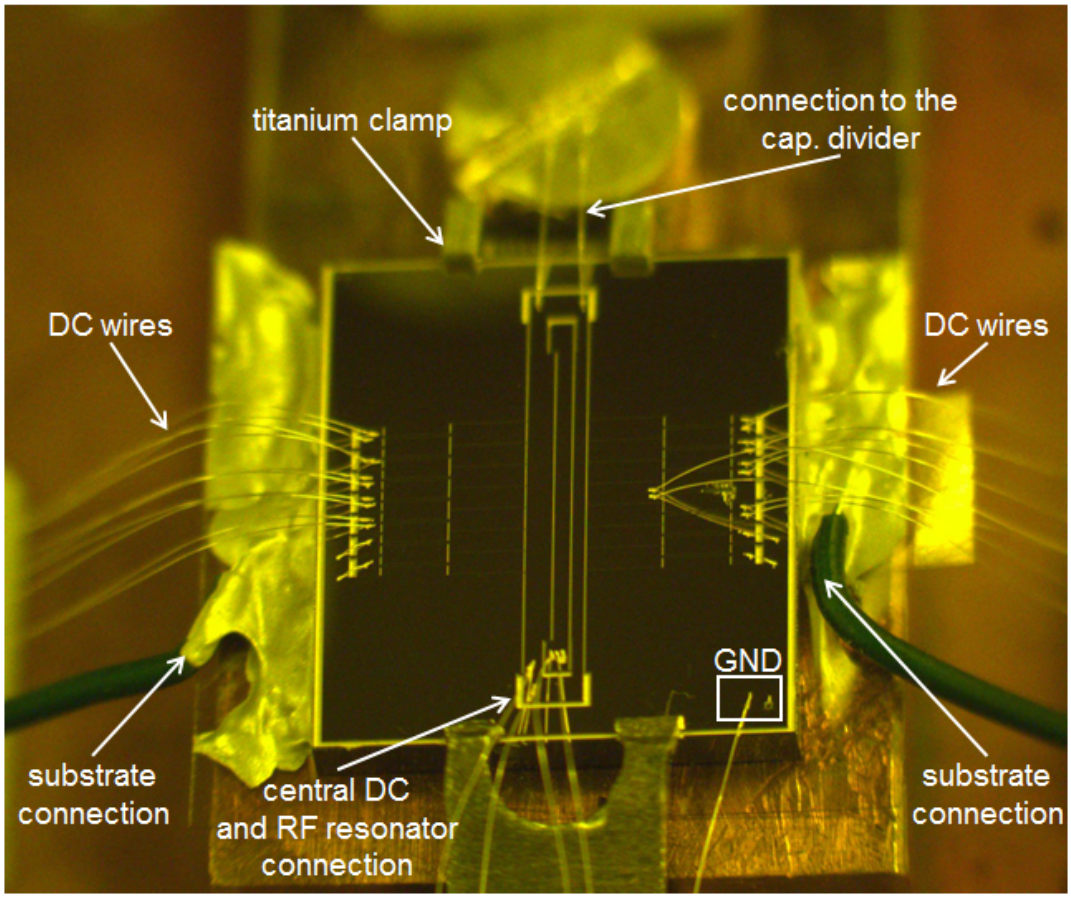


Figure 7.1: Yedikule trap, mounted on the copper carrier after wire bonding. The bonds are made of gold and have a diameter of 25 µm. The trap is fixed by titanium clamps which are bolted down to the copper carrier by brass screws. The trap has an additional connection to the substrate which allows us an in situ measurement of the resistivity or to apply a DC bias to the substrate. Figure courtesy of Kirill Lakhmanskiy.

Once the trap is mounted and placed inside the vacuum chamber, the chamber is closed and a turbomolecular pump is connected. A heater is used to heat up the 10 K stage to 320 K which helps to reduce the amount of water inside the system and to speed-up the pump-down process. The pump reduces the pressure to a value of $< 10^{-6}$ mbar which takes roughly one day. At this point the cryostat is switched on to cool the system. The

heater is switched off when the 50 K stage reaches a temperature of 240 K. This prevents the residual water from freezing on the trap surface, as the trap is not the coolest surface inside the chamber. The final temperatures of the stages are 50 K and 6 K, respectively. It takes roughly 350 minutes of cooling to reach these temperatures [23].

After the cooling-down procedure, the voltages are applied and the lasers need to be aligned. For trapping, four lasers are needed: The photo ionisation of ^{40}Ca is a two-photon process where two lasers are used. The 422 nm laser is resonant to the $4^1S_0 - 4^1P_1$ transition and the 375 nm drives the transition from 4^1P_1 to the continuum [100]. The 397 nm laser is used to Doppler cool and detect the ion. This procedure also requires repumping at a wavelength of 866 nm (see section 2.4).

The laser beams are overlapped before entering the vacuum chamber and are observed with an EMCCD camera. The beams share one lens, which makes it easier to adjust their direction simultaneously without changing their alignment with respect to each other. A micrometer screw allows us to do the adjustments in a controlled manner. The laser beams are directed to hit the trapping site. Once the position of the lasers seems reasonable, the oven is switched on which creates a continuous flux of calcium atoms. The micrometer screw is used to scan the position of the laser beams in a small region around the trapping site, until the first ion is trapped. The trapping success can be observed by an EMCCD camera, which collects the fluorescence light from the ion. The EMCCD image of the first trapped ion by a Yedikule trap fabricated by Infineon Technologies is shown in figure 7.2.

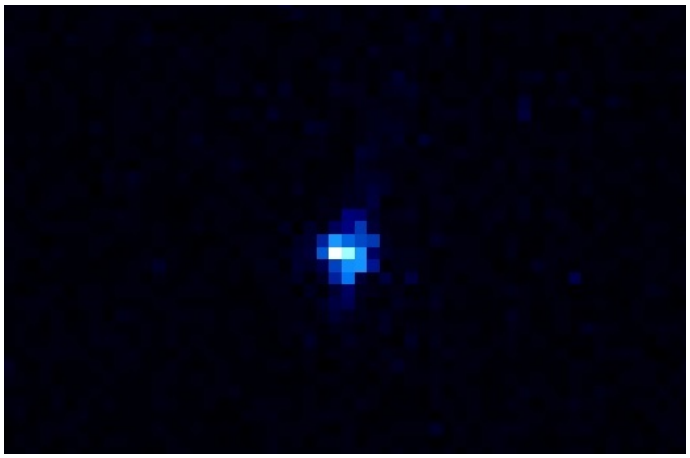


Figure 7.2: EMCCD image of the first trapped ion by a Yedikule trap fabricated by Infineon Technologies. Image courtesy of Kirill Lakhmanskiy.

The trapped ion indicates the right position of the laser beams. With an ion in the trap, the oven is switched off and the two lasers for ionisation are physically blocked. The next step is to minimize the micromotion and to start with measurements. An important physical quantity is the heating rate of the traps. In the following, the corresponding measurements and results are shortly summarized.

7.2 Heating rate measurement

The measurements use sideband spectroscopy as described in subsection 3.2.3. On three consecutive days the heating rate is repeatedly determined. In order to investigate a possible influence of the electric potential of the substrate, the DC bias is varied. The data is taken with a single ion, on the axial mode with an ion-surface distance of 230 µm and trap frequency at 1 MHz. Table 7.1 summarizes the results.

day	DC bias	$\dot{\bar{n}}$ $(quanta/s)$
#01	floating	731 ± 260
	GND	378 ± 141
	+10 V	809 ± 112
#02	floating	459 ± 50
	GND	291 ± 50
	+10 V	434 ± 61
	−10 V	581 ± 75
	−15 V	1170 ± 187
#03	+5 V	464 ± 86

Table 7.1: Values of the heating rate, measured by sideband spectroscopy. The data are taken on three consecutive days. The measurements where carried out by Kirill Lakhmanskiy.

The lowest measured heating rate for this trap is $\dot{\bar{n}} = 291 \pm 50$ quanta/s, measured on the second day with grounded substrate. The value for the same measurement with a floating potential of the substrate measured at the same day is $\dot{\bar{n}} = 459 \pm 50$ quanta/s. Increasing the bias voltage to ±10 V yields higher heating rates, which is also the case when the potential of the substrate is floating. This differences indicate an influence of the potential of the substrate on the heating rate. The same behaviour can be seen in the data from the first day, but here the heating rates are generally higher.

The highest heating rate, $\dot{\bar{n}} = 1170 \pm 187$ quanta/s is for a bias of −15 V, measured on the second day. The measurement with +15 V yields no result because of poor sideband cooling or excessive heating rate. The same is true for the measurements from the third day. Here only the measurement with +5 V gives a reasonable value. In general, significant day to day fluctuations of the heating rate can be observed. These fluctuations are not understood and need further investigations.

There exist various theories about the origins of heating [48, 101]. One reason for the positive influence of additional grounding of the substrate may be the thick thermal oxide layer that we use for the fabrication. This layer, as it is thermally grown, covers also the backside of the wafer and therefore the backside of every single chip. This oxide layer might prevent the substrate from being grounded by the trap mount. The wires for the additional grounding are applied to the sidewalls of the chip, where the thermal oxide layer is not present. This hypothesis may be checked by removing the oxide on the backside of a wafer or on individual traps. More details about these measurements will be given in Kirill's PhD-thesis.

The determined heating rates can be compared to to those of Michael Niedermayr's experiments. Over a period of six weeks, he measured the heating rate of one trap several times. The trap design was the same as for the measurements done here. The determined heating rate from different measurements over a period of six weeks yielded a value of $\dot{\bar{n}} = 0.6 \pm 0.2\,\text{quanta/s}$, which is significantly lower than the recent results reported here.

It is difficult to figure out, what the differences between the traps and experiments are that could lead to such deviations of the heating rates. One point might be the difference in the treatment of the trap surface after metallisation: Michael Niedermayr did the gold evaporation in the university's cleanroom as the final step of the fabrication. The Infineon traps where diced and transported after metallisation, without a special protection of the surface. It is reasonable to think, that the conditions of the surfaces differ and therefore contribute to the strong deviation between the measured values. In order to be able to identify or exclude impure surfaces as a possible cause for the high heating rates, experiments with traps with a lower trapping height would be interesting. For such cases, however, the influence of scattered light can be higher as the lasers are aligned closer to the traps surface and thus also can influence the heating rates. It is crucial to prevent the substrate from direct exposure to the laser light, because all the used lasers are capable of creating electron-hole pairs in the substrate. The way how such local charge carriers could affect the experiments is discussed in the following.

7.2.1 Influence of stray light with silicon as a substrate

Photons from the lasers that hit bare silicon areas can cause the formation of electron-hole pairs. Due to local changes of the conductivity of the substarte, RF losses might increase and therefore harm the experiments. The electrode-ion separation in the presented experiments is around 230 µm. The produced traps include scaled versions with a reduced trapping height, namely 150 µm, 100 µm and 50 µm. To further investigate the observed heating, it would be interesting to test some more of the Infineon traps. These tests could involve experiments with some of the scaled traps, which operate at a smaller trapping height. Experiments with ions closer to the surface would include the need of aligning the lasers closer to the surface. Such alignment could cause more light to be scattered at the traps surface. The scattered light leads to the creation of electron-hole pairs in the silicon substrate [102]. The trap's surface is covered and protected by the gold layer, but the sidewalls of the trenches and the chip provide bare silicon or silicon oxide. The band-gap of silicon at 10 K is 1.17 eV, which corresponds to light with a wavelength of 1061 nm [103]. All the lasers used during the experiments have a shorter wavelength and provide enough energy to create electron-hole pairs. Such charge carrier generation could be one reason for the observed day to day fluctuations of the heating rate which would get even worse for the scaled traps.

The trap design of the 2D linear trap arrays presented in Chapter 4 already addresses the problem concerning charge carrier generation inside the substrate. The first metal layer covers almost the whole chip surface and is kept at ground potential. This grounded layer serves as a barrier, which eliminates the influence of local charges inside the substrate

on the experiment and also as an optical shield. The drawback of this shielding layer is a significant increase of the capacitance of the RF electrodes to ground. Therefore, the reticles contain different trap versions with different capacitance, as some traps have a first metal layer which is partially removed underneath the RF electrodes. The calculated capacitances are 24.7 pF and 12.1 pF. The higher the capacitance of the trap, the more RF power is needed to operate the trap. In comparison, the YK traps have a capacitance of $5 - 9$ pF.

Besides shielding the substrate, it would be possible to reduce the amount of stray light. As a result of the fabrication, described in section 5.4, the surface of the trap shows a surface height variation of up to 4 µm. This surface is schematically shown in figure 7.3. The topology, together with a trapping height of 120 µm or 80 µm, can cause more stray light than a comparable planar surface. Depending on whether stray light harms the experiments, reducing the topology at future trap fabrication by changing the workflow to other processes might be necessary.

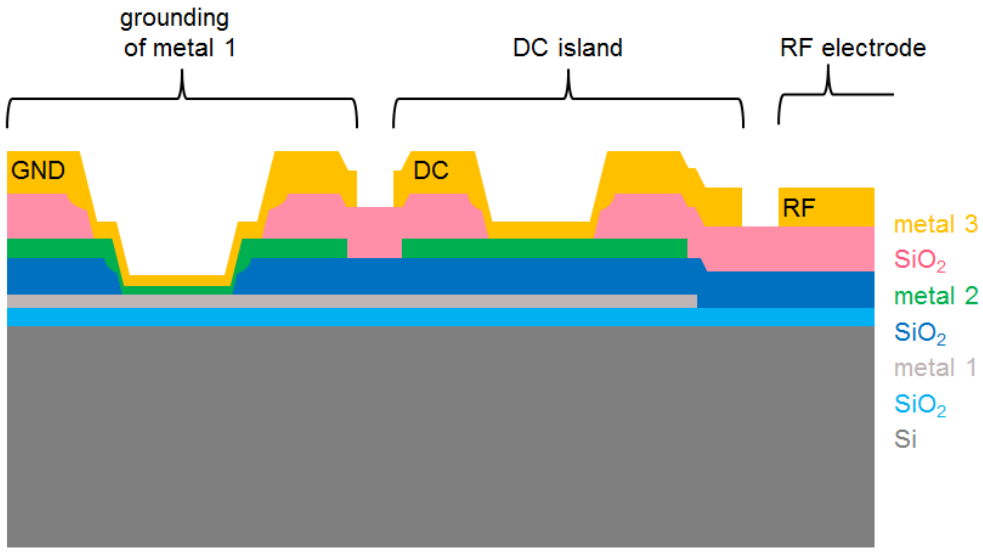


Figure 7.3: Schematic of the surface of the 2D linear trap arrays. Three examples of topology: The strongest topology arises from vias which connect the first and the third metal layer for grounding (via-in-via). Here the topology is around 4 µm. The topology for DC islands is special as those electrodes are the smallest once and the most of them are equipped with two vias. Therefore, the vias make up almost a third of the electrode area. For some versions, the first metal layer is removed underneath RF, which also increases the topology.

The surface height variation (topology) arises from the structured layers underneath the third metal layer. Especially vias which connect the first and third metal layer (via-in-via) contribute regions of strong topology (up to 4 µm surface hight variation). The deposited oxide layers copy the topology given by the underlying layers or make it even stronger for the upcoming once. Due to the topology, the stray light is scattered differently compared to planar trap surfaces. The topology could be smoothed by a variation of the deposition processes. There are processes available which are a combination of deposition and back-etching. The deposition of a far thicker oxide layer and its follow-up back-etch would smooth the topology, which benefits follow-up lithography steps. It is easier to have a

uniform resist thickness all over the wafer, if the topology is smoother.

A way how to completely remove the surface height variations is to use vias which are filled with tungsten. There exist processes, where the vias are opened and filled with tungsten, followed by chemical-mechanical polishing (CMP). This leaves the surface almost planar. However, these processes are more complicated and more expensive, but depending on the necessity of reducing the topology it might be reasonable to implement them.

Chapter 8

Conclusion

Surface ion traps are a very promising way towards scalable quantum computers and quantum simulators that operates with trapped ion. This work provides the first steps towards the industrial production of ion traps at Infineon Technologies in Villach. For two individual trap designs, workflows have been developed and implemented in a sustainable way, such that new wafers could be directly started and fabricated with the same process scheme without any extra effort. The corresponding individual processes have been selected in close cooperation with many process experts.

The first design "Yedikule" was already known and tested by a former PhD-Student of the group and served as a first test run for the fabrication at Infineon Technologies. Continuous quality control enabled the successful fabrication on two different base material types on 8" wafers. A final failure analysis, including a cross-section analysis and an electrical test of the trap structures, confirmed the quality of the traps. In total, seven wafers, which corresponds to roughly 5300 single chips, where delivered to Innsbruck for further characterization. The lowest determined heating rates was $\dot{\bar{n}} = 291 \pm 50$ quanta/s, but we observed day to day fluctuations of around 100 quanta/s. The origins of the high heating rate and of its fluctuations are not clear yet and require further investigation beyond the scope of this thesis.

As the second trap design, 2D linear trap arrays for quantum simulations where developed. For these traps, simulations enabled optimization of the design, which uses three structured metal layers with vias. The fabrication of such a trap already exceeds the horizon of the fabrication possibilities in the university clean room. Therefore, these traps represent the first tremendous benefit, resulting from the cooperation between the University of Innsbruck and Infineon Technologies. By the end of my work, a whole new set of reticles could be drawn and ordered, which includes six different versions of the target trap design. These reticles, together with a corresponding workflow, are implemented in such a way, that everything is ready for the fabrication which has already started.

As a direct result of my master's thesis, Infineon Technologies together with colleagues from the University of Innsbruck, the ETH Zürich and I-FEVS [1], participated in an EU funding application. This application was evaluated positively. The corresponding resources enable

[1] Interactive Fully Electrical Vehicles SRL, Italy

the follow-up project "PIEDMONS" [2] which includes five PhD students. Thus, my Master's thesis has indeed laid the foundations for further cooperation between the University of Innsbruck and Infineon Technologies.

[2] Portable Ion Entangling Devices for Mobile-Oriented Next-generation Semiconductor-technologies

Outlook

New trap fabrication capabilities

The available processes of Infineon Technologies can be used to improve micro-fabricated ion traps. The fabrication capabilities enable such highly complex trap designs, that could not be manufactured in a university cleanroom. 3D traps built at universities typically consist of multiple components that are screwed [104] or glued [105] together. At Infineon Technologies, these multiple components can be bonded together with a precision that cannot be achieved by such manual assembly techniques. Higher precision will decrease axial micromotion induced by manufacturing imperfections. The achievable alignment accuracy for wafer bonding is in the sub micron range, which suits the needs of trap fabrication. 3D traps are interesting as they offer much deeper trapping potentials compared to 2D traps, which is an advantage for operating the trap at room temperature. Room temperature experiments have more residual gas in the chamber and the atoms and molecules have more energy. Therefore, collisions between the ion and the gas are more problematic than with comparable cryogenic setups. The deeper potential of the 3D trap prevents the ion loss due to collisions and would therefore allow the operation at room temperature. A schematic of a 3D trap formed by wafer bonding is shown in figure 8.1.

For this schematic trap design a total of three wafers needs to be bonded together. The top and bottom wafer carry the electrodes, whereas the intermediate wafer serves as a spacer and contains the bonding pads for the electrodes of the top wafer. The top wafer has an etched hole to provide more optical access. The given dimensions are rough estimates of what might be possible from the process point of view. Depending on the actual trap design and the wafer materials, eutectic bonding between two gold layers or anodic bonding between silicon and fused silica could be used for the fabrication.

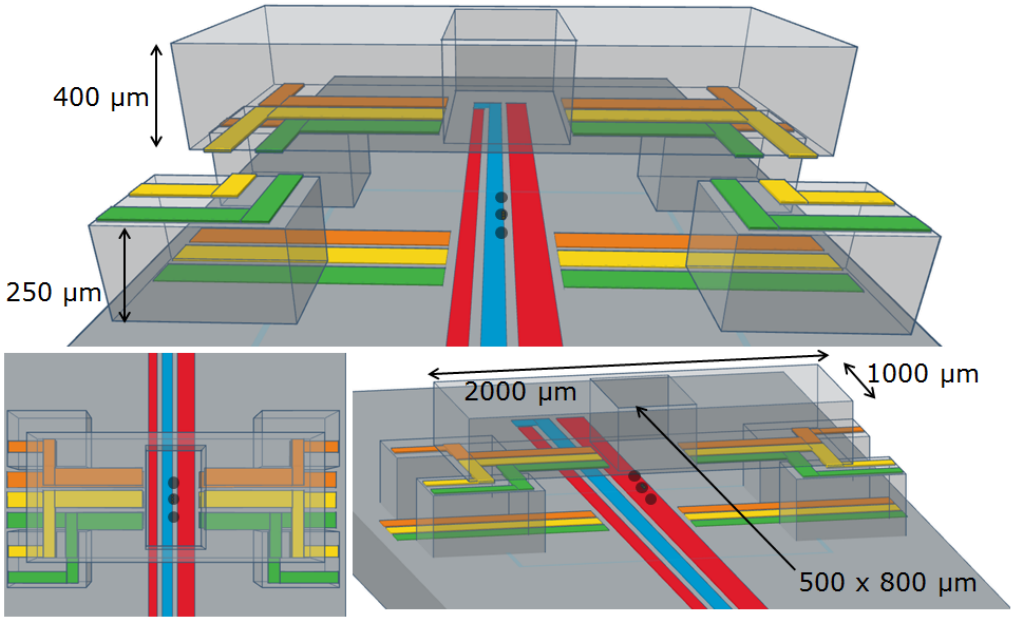


Figure 8.1: Schematic of a three-dimensional on chip ion trap formed by wafer bonding. Three wafers are bonded together: The top and bottom wafer carry the electrodes to confine the ions (orange, green, yellow). The intermediate wafer serves as a spacer and contains the bonding pads for the electrodes of the top wafer. The top wafer has an etched hole to provide more optical access. The ions are indicated by the black balls. The given dimensions are rough estimations.

The increased complexity of such a trap demands new concepts in terms of optical access. The integration of wave guides for addressing the individual ions might be necessary. There exist already experiments where this was implemented successfully [106].

A general way to improve future ion traps, independent of whether they are two- or three-dimensionally structured, is to integrate electronics directly on the chip. Especially for filter electronics it is very important to place it as close as possible to the trapping electrodes. The shorter the wires between the filter and the electrode, the better the DC electrodes are shunted to RF ground. Residual RF on the DC segments influences the confinement and causes axial micromotion [107]. Besides filters, the integration of analog switches or analog-to-digital converter (DACs) could be interesting. By integrating DACs, fewer cables need to be routed into the vacuum chamber, which would increase the number of independent voltages that can be used during the experiment. The use of more DACs would improve the experimental capabilities, as more DC segments can be controlled. This is particularly interesting for experiments where ions are shuttled across the chip [108].

Appendix A

The two reticles used for the fabrication of Yedikule traps, called G2060-A and G2060-B, are shown in figure 8.2.

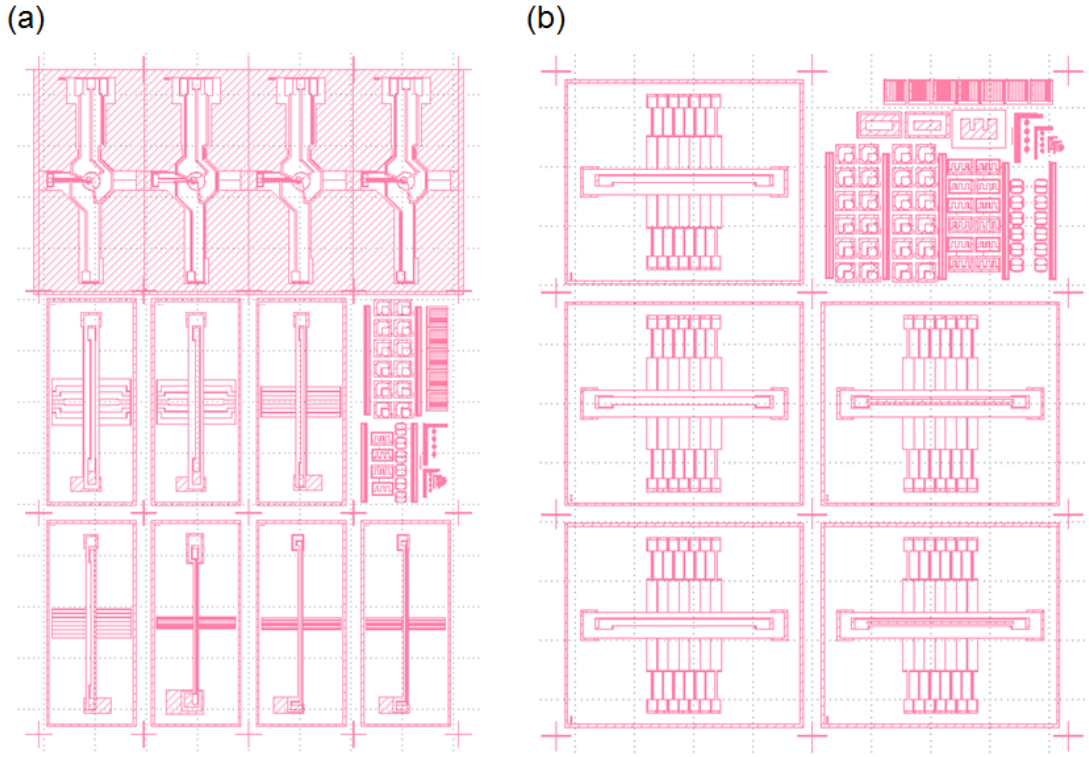


Figure 8.2: The two reticles for the Yedikule fabrication. **(a)** Reticle G2060-A. **(b)** Reticle G2060-B.

Besides different scaled versions of the actual YK design, they contain test structures for resolution tests. The reticle G2060-A includes so-called "point traps", which can be seen in the top row of the reticle's picture. These point traps are designed to measure the heating rate as a function of the trapping height. A more detailed picture of one test structure and point trap is shown in figure 8.3.

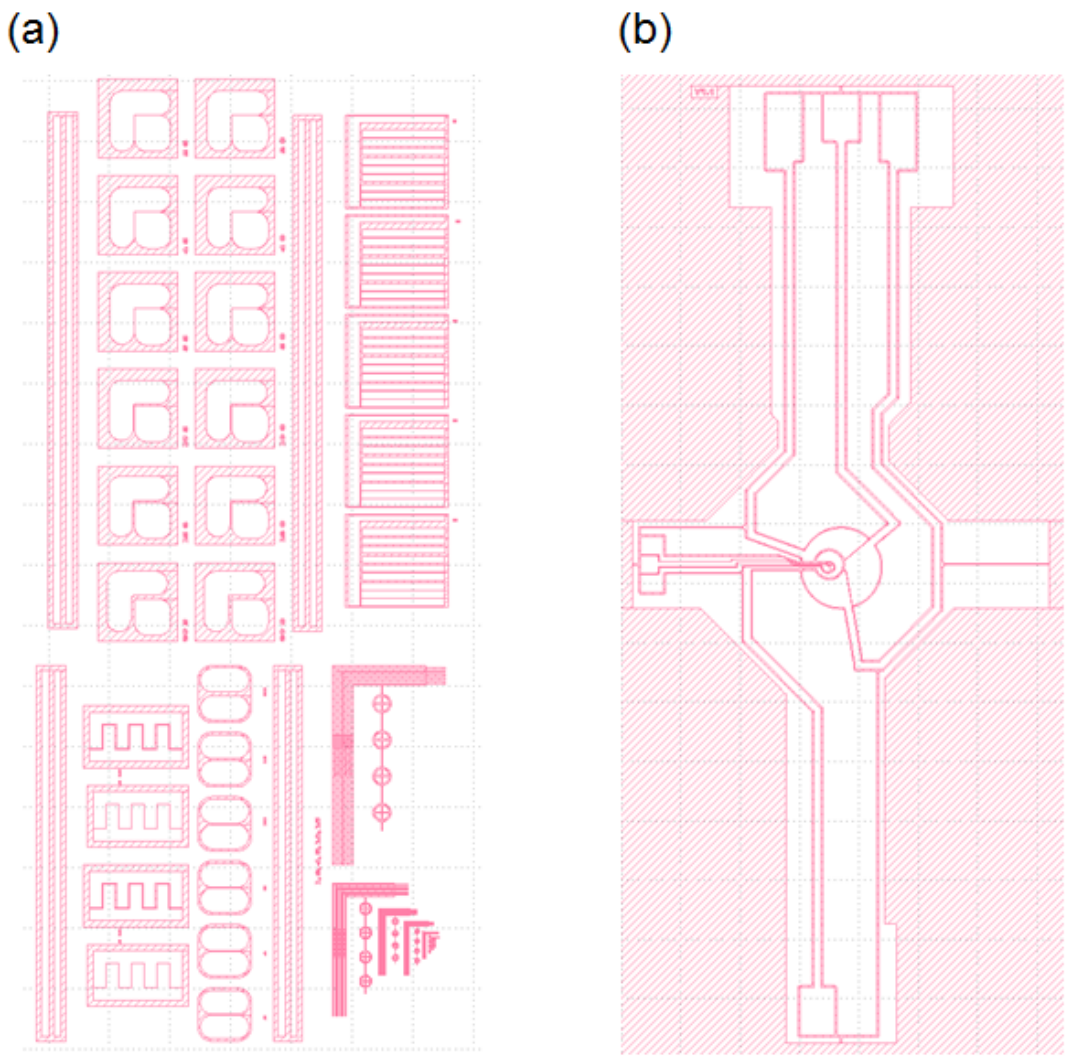


Figure 8.3: Details of reticle G2060-A. **(a)** Structures for resolution tests. **(b)** Point trap to measure the heating rate as a function of the trapping height.

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